Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp287-288

High Heat Flux Dissipation Via Interposer Active Micro-Cooling

Federico Buja[1], Lei Zhang[1], Vladimir Cherman[1], Herman Oprins[1], Ben Jones[1] and Philippe Soussan[1]

[1] IMEC
Kapeldreef 75, 3001
Heverlee, Belgium
Phone: +32 16 28 87 04 E-mail: federico.buja@imec.be

Abstract

In this work we demonstrate that high power density of 600W/cm^2 can be effectively dissipated by conductive/convective cooling using an interposer with integrated micro-channels. This technology proved to limit the temperature increase of a 5mm^2 power chip to only 34K when operated at 150W. The cooler technology is developed on a silicon semiconductor platform and is applicable to interposer technologies.

1. Introduction

The scaling of integrated chips is continuing at a fast pace, therefore resulting in an ever increasing power density with obvious repercussions on the functionality and performances of the devices.

Power dissipation can find great benefits with chip-level liquid cooling. A microfluidic heat sink can lead to a greater thermal dissipation between an IC chip and the convective cooling medium.

The heat transfer enhancement using micro-channels has been reported [1] and thoroughly simulated with detailed analysis [2]. Many advanced cooling solutions have been explored and several fundamental technological development have been studied [3].

With this work we report on the fabrication and testing of a cooling micro-device with the capability of dissipating a power density of 600W/cm^2, leading to a temperature increase rate of 0.22K/W in the power test chip. This is obtained by conductive/convective phenomena using ambient temperature water as a cooling medium. The simulations and measurement performed [4] demonstrate how the integration between a power chip and a micro-fluidic platform can be a promising solutions for dissipating high power density.

2. Fabrication process

The fabrication of the micro-fluidic platforms is divided in two parts: the etch of the cooling micro-channels (prior fusion bonding) and the full chip fabrication (post fusion bonding). To achieve these two types of micro-devices, two different approaches are adopted. For a direct cooling of the power test chip, we adopt a configuration called “open channels” (OC), while for a conductive type of cooling we use a “close channels” (CC) configuration. In Fig.1 the two types of assemblies are reported.

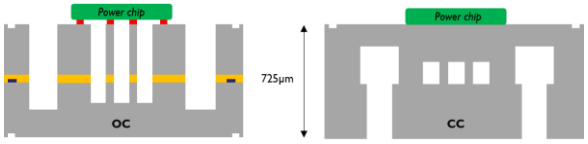

Fig. 1 - Open and close channels configurations.

The key process, common to both configuration, is oxide-oxide fusion bonding. Starting from a standard, 8” silicon wafer, a 100nm tungsten (W) layer is patterned for the definition of a zero layer, needed especially for infra-red (IR) alignment after fusion bonding. A CVD oxide is then deposited, sintered and thinned down to 350nm via chemical mechanical polishing (CMP). It is fundamental to obtain the lowest possible roughness, to guarantee a smooth fusion bonding process.

The OC and CC patterns are then transferred onto the oxide layer, via an IX type resist, with a thickness of 4500nm. This resist budget is optimized to sustain the following deep reactive ion etching (DRIE) process, needed to carve the micro-channels into the silicon, to a depth of at least 150µm. Of paramount importance is that the oxide is never exposed to the etch species, to avoid an otherwise increase in roughness. An oxygen plasma strip followed by a wet residues removal bring back to surface to pristine conditions for fusion bonding. Also this process is common for both micro-devices, since the bonding is carried out with a bare silicon wafer, with 100nm thermal oxide grown onto its crystalline surface. After curing the bonded couple and grinding both sides, we obtain a 725µm standard thickness wafer, that can be easily processed in any CMOS compatible FAB equipment. To continue the fabrication for the OC micro-devices, via IR alignment, a 3-5 µm Cu-Sn layer is plated on the silicon. Finally, a 30µm thick resist is patterned to conformally cover the solder layer and allow the DRIE of the open channels. When landing on the previously etched channels they will guarantee a direct contact between the fluid and the power chip.

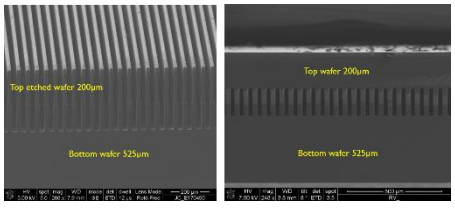

Fig. 2 – Scanning electron micrograph of OC and CC respectively.

The CC devices, are obtained instead with a simpler process: only one DRIE etch is needed on the wafer backside to create and inlet and outlet for the fluid to enter the channels.

In parallel to the cooling devices, a power test chip was fabricated, using a 350nm tungsten layer designed to deliver a at least 150W on an area of 5mm^2. This design is implemented in order to meet the required power density of 600W/cm^2. Below the active layer, a 300nm SiN insulates the substrate and above the W, a 1µm thick AlSi is patterned to provide the contacts for the wire bonding. Utilizing a temporary bonded carrier, the wafers are finally ground to a thickness of 100µm, and the backside plated with a Cu or Cu/Sn layer. The 3D assembly of the power test chip and the microcooler is carried out by means of thermo-compression bonding (TCB), at a minimum temperature of 270ºC (Fig. 2).

Fig. 3 – Photo of the final TCB between the OC and power test chips.

2. Measurement results

The power test chips are bonded to the OC and CC microcooling devices using the same conditions and metal stacks, in order to obtain a common base line to compare their characteristics. The bonding interface is always composed by Cu (3µm), Sn (5µm) in contact with Au (500nm). A 10nm seeding layer of Ti is used on both sides to improve adhesion between the metals and the silicon.

In Fig. 4 are reported the experimental results of the cooling performances obtained by using OC or CC devices with the power test chip. In OC configuration the maximum power of 150W is achieved, while for CC, due to wire bonding issues, the maximum power tested is 72W. The width of the channels for both cases is 30µm, with a depth of 350µm and 150µm respectively for OC and CC. At the maximum tested power we observe a temperature increase of 34K for the test chip when cooled with OC, and 28K when cooled with CC.

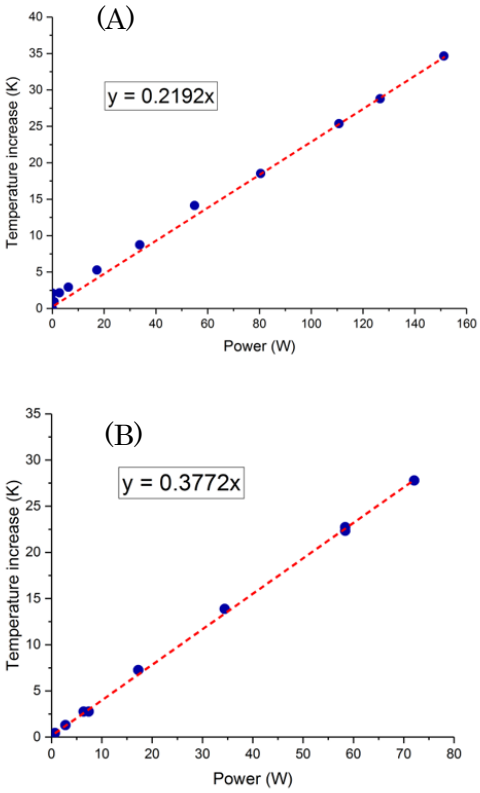

Fig. 4 – (A) Power test chip temperature increase when bonded to OC. A pressure of 1.8bar and a flow rate of 150ml/min are applied; (B) Power test chip temperature increase when bonded to CC. A pressure of 2.3bar and a flow rate of 143ml/min are applied.

3. Conclusions

We have described in this paper a novel approach for effectively dissipate a high power density of 600W/cm^2 by means of integrated micro-channels technology realized on a silicon platform using direct wafer bonding. This lead to a maximum temperature increase of the power chip in operation of only 34K. The optimization of this technology is therefore promising for advanced packaging of ever increasing power densities in IC components .

References

[1] A. Dewan and P. Srivastava, Journal of Thermal Science. **24** (2015) 203-214.

[2] W. Qu and I. Mudawar, International Journal of Heat and Mass Transfer. **45** (2002) 3973.

[3] S. Kandlikar, Heat Transfer Engineering. 26(8) (2005) 5-14.

[4] L. Zhang *et al.*, High heat flux removal using optimized microchannel heat sink, submitted to Therminic (2018).