Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp289-290

Embedded Multiple-Time Programmable Memory by BCD Process for High Voltage CMOS Circuits

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Abstract

In this paper, a floating gate MTP cell implemented by BCD (Bipolar/CMOS/DMOS) process for high voltage integrated circuits was presented. This specially-designed, full-CMOS-compatible cell employing a standard gate dielectric layer are electrically programmed and erased by bi-directional FN tunneling operations. Featuring low-power consumption and reliable data retention and exceptional cycling endurance, this MTP technology can be a highly feasible candidate for reliable CMOS compatible NVMs for HV circuits.

Introduction

In the IOT era, many embedded technology become increasing important and critical to the implement of small and compact IC modules with extended functionalities. More functions are combined in a single chip (System on Chip; SoC) to deliver higher performance at lower cost [1-2]. As technology advances forward, SoC solutions involve greater design complexity and more sophisticated features [3], such as adaptive setting, smart sensing, etc. BCD technology, see in Figure 1, can be highly integrated to CMOS logic modules for SoC solution. This technology allows MOS devices to sustained high-voltage (HV) are widely used in mobile and communication applications [4]. In these HV circuits, NVMs (non-volatile memory) are an indispensable part when fine-tuning of parameters and smart or adaptive functions are increasingly in demand [5]. Embedded NVMs with good compatibility and exceptional reliability even under the severe environments becomes one of the key modules in ICs for the automotive and industrial applications [6]. Challenges differ for NVM developments as CMOS technologies diversified [7]. In this work, a MTP based on a BCD technology is proposed for high voltage IC systems. Low-power consumption, exceptional cycling /data retention characteristics as well as disturb immunity, has been demonstrated with this full-compatible MTP solution.

Cell Structure and Operation Principle

The proposed MTP cells investigated in this study is fabricated by 0.18μm single poly-Si BCD process. As shown in Figure 2, the poly-Si floating gate (FG) is laid on top of two isolated n-well regions as the program gate (PG) and the erase gate (EG), and a read transistor channel. The storage data in the floating gate can then be read out through the BL current via a select transistor controlled by the wordline (WL). The cells are arranged in a NOR-type array, as shown in Figure 3, where selection/inhibit of a cell is controlled by PG, BL and WL. EG are shared for cells in the same block, so that block-erase can be achieved.

To enable programming of a floating gate cell, electron can be injected into a FG either by CHEI (Channel Hot Electron Injection) or by Fowler-Nordheim (FN) tunneling. In most circuits, the high voltage required for FN tunneling can lead to reliability challenges for peripheral circuits, such as decoders as well as charge pump circuits. Here, HV devices are readily available in BCD technology, hence, will not be a key concern. In addition, the used of n-well region as the HV nodes (PG and EG) enables voltage tolerance for the operation of this cell. Through well coupling, floating gate potential can be controlled to allow erasing and programming by FN tunneling operation. (Figure 4(a)(b)) The coupling ratio of PG is maximized to increase programming speed. As shown in Figure 5, PG area is designed to be much larger than that of EG. The channel FN tunneling is enabled for programming when proper selection voltage applied. Data in Figure 6(a) suggests that a higher bias V_{EG} slightly increases V_{FG}, consequently, effectively raises its programming speed. As revealed in Figure 6(b), an optimal voltage at approximately 8V can enhance programming speed while avoid program disturb on unselected cells. For erase operation, higher potential difference can be easily established between FG and EG, as the EG coupling ratio is minimized. The time-to-program and erase characteristics at different operation voltages are compared in Figure 7. Here, we set the program state and erase state at threshold voltage of 1V and of -2V, respectively. As shown in Figure 8(a), V_{PG} is set to 0 during read. The positively charged FG can turn on the channel in erase state, so that a bit-cell current is read as the corresponding WL is turn on. Figure 8(b) shows that a bit cell current > 60μA can be readily obtained.

Reliability Evaluations

For endurance testing, the threshold voltage of program and erase states are monitored during P/E cycling. The test results arranged in Figure 9 reveal that the sensing window remains larger than 2V even after 10^5 P/E cycles. Program disturbance can be critical for cell programmed by channel FN. Disturb characteristics on cells sharing a common PG shown in Figure 10 suggests that a 8V inhibit voltage on BL are sufficient to prevent unselected cell from changing state. Namely, a maximum number of 1K cells can share the same PG. For data retention tests at temperatures of 150℃ and 200℃ are performed. The chosen program state is very close to the neutral state of this cell, charge loss is not significant during data retention test. On the other hand, the positively charged FG can induce charge gain, leading to a positive shift in threshold voltage. As illustrated and observed in Figure 11, slightly shift during charge gain did occur after baking for 100 hours at 200℃. Read disturb test in Figure 12 projects that under the current read condition, this cell can be read continuously for well over 10 years without read error.

Conclusion

A HV MTP memory based on BCD process is demonstrated. With low-power consumption, high-voltage toleration and good reliability performance, this MTP memory is suitable for future embedded NVM memory for high-voltage circuit applications.

References

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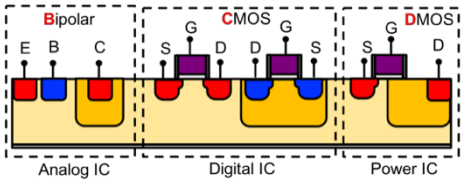

Figure 1 By integrating three distinct components on a single die, BCD (Bipolar/CMOS/DMOS) technology help to reduce the cost in BoM (bill of material).

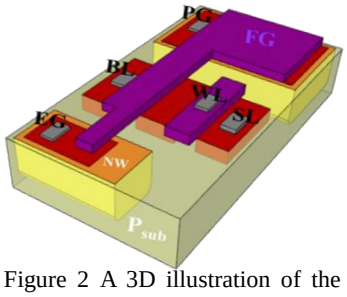

Figure 2 A 3D illustration of the proposed single-poly MTP cell.

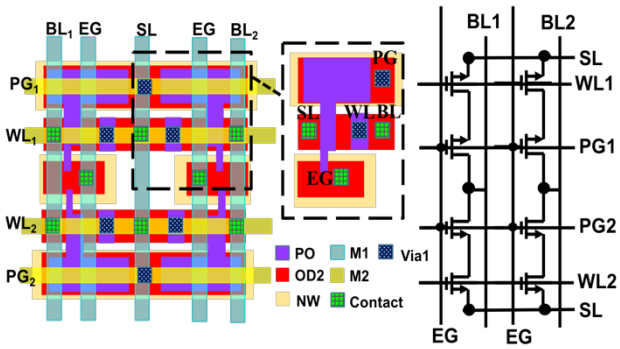

Figure 3 The 2x2 NOR-type array layout and schematics are shown.

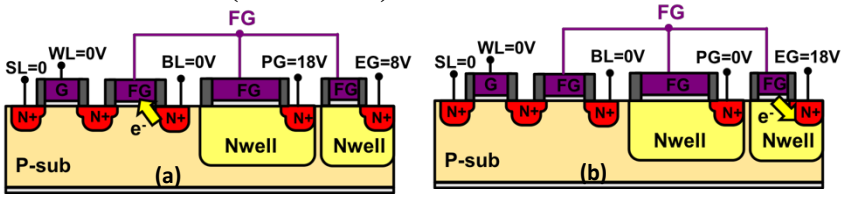

Figure 4 By using well coupling to control the floating gate potential, this MTP cell can be erased and programmed by FN tunneling. (a) FN-program. (b) FN-erase.

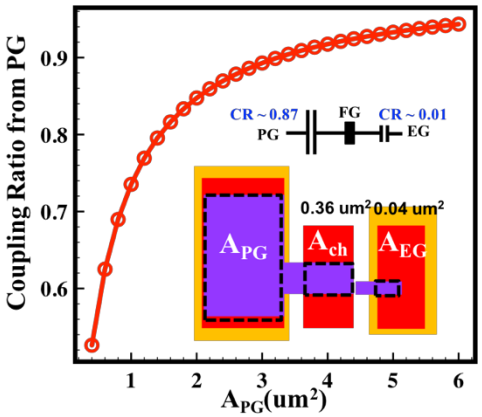

Figure 5 Coupling ratios of PG and EG can be designed flexibly by adjusting the overlap area between FG and the corresponding gates.

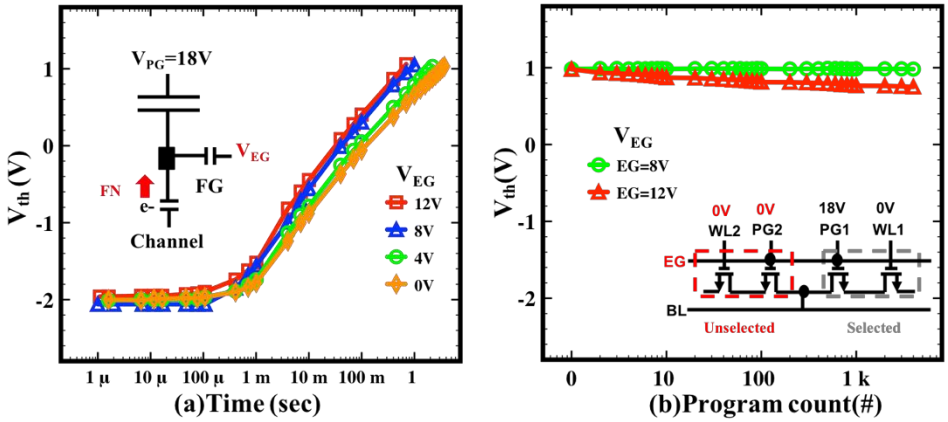

Figure 6 (a) Increased V_{EG} raises the FG potential, and increases programming speed, as expected. (b) When EG is at 12 V, the program disturb is observed, the unselected cell can be erased slightly during program. Lowering V_{EG} 8V can effectively relieved this problem.

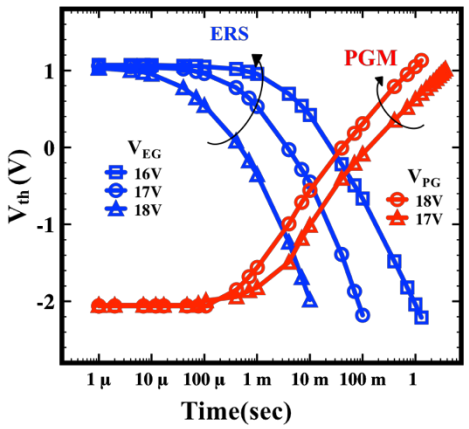

Figure 7 Time-to-program and time-to-erase characteristics demonstrating a programming period within 800msec and erasing period of less than 10msec.

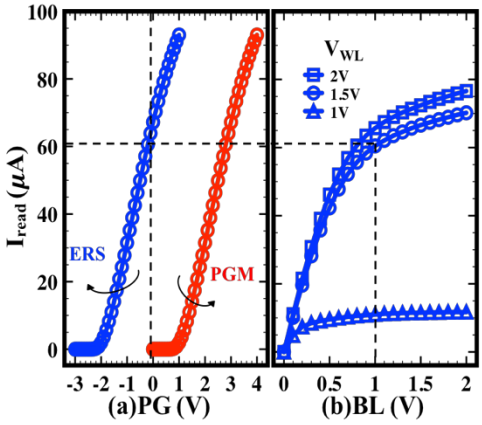

Figure 8 (a) I_D-V_{PG}. (b) I_D-V_{BL} with different WL condition. Under a reading condition of PG=0V, WL=1.5V, BL=1V, the sensing bit cell current can exceed 60 μA.

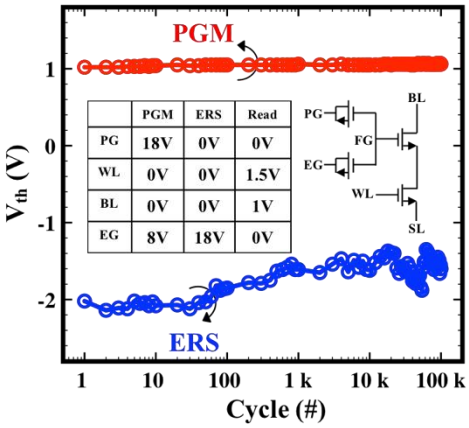

Figure 9 After 100K P/E cycles, the sensing window can remain larger than 2V. The operation table and schematic of cell are summarized.

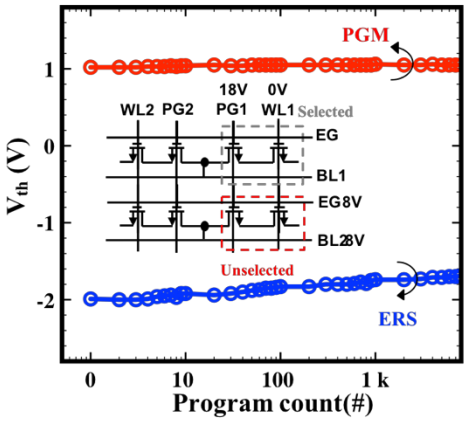

Figure 10 After more than 1k pulse stress, program disturb is effectively alleviated with an inhibit voltage of V_{BL}=8V on the unselected string.

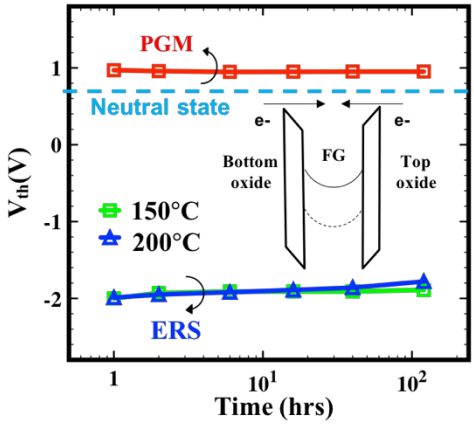

Figure 11 Data retention characteristics of the MTP cell baked at 150°C and 200°C, respectively. Slight charge gain is observed after 100 hours of bake.

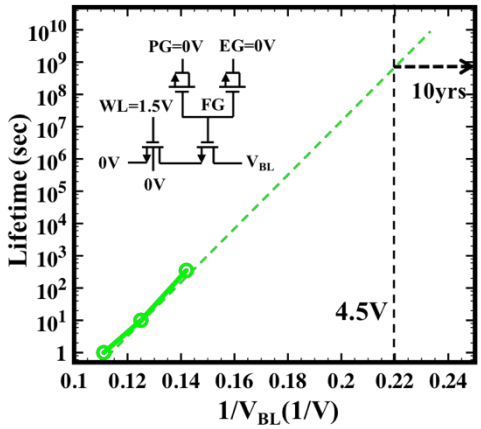

Figure 12 Read disturb projection reveals that the cell can be continuously read for over 10 years without exceeding the failure criteria of I_{read} < 1n A.