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Operation of Basic Logic Element in 3D Structure Using BEOL Transistor with In-Zn-O Channel Offset for Power Management Integration Circuit

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Abstract

In this study, we fabricated thin-film transistors (TFTs) using In-Zn-O (IZO) film as channel layer on the back end of line (BEOL) of silicon wafers (silicon IC fabrication) for power management integration circuits (PMICs) and implemented resistor-type inverter circuit by applying drain offset channel. The IZO BEOL transistor was fabricated by a heat treatment process at a temperature lower than 400 °C to prevent degradation of chip reliability, and showed a high field effect mobility of 27.36 $cm^2/V{\cdot}s$ and a low interface state density (D_{it}) of 2.68×10^{12} $cm^{-2}{\cdot}eV^{-1}$. In addition, the IZO inverters, the fundamental building block of logic circuits, were implemented using a drain offset structure and showed stable inverter characteristics. Therefore, IZO BEOL transistors and drain offset inverters allow monolithic three-dimensional (3-D) integration of the transistor into the BEOL of silicon wafers for PMICs and functional circuit device applications.

1. Introduction

Recently, electronic devices and components require high efficiency energy saving types due to environmental problems and energy supply problems [1]. Thus power devices and large scale integration (LSI) are becoming important research issues because they are an important part of creating an energy saving society. As CMOS technology shrinks, power supply voltages are reduced to ~1 V for low power consumption, but many devices such as automotive electronics, displays and consumer electronics still require high-voltage operation. Therefore, on-chip bridging I/O devices between high-voltage and low-voltage devices for micro-controller-units (MCUs) are becoming important. In this study, BEOL transistors were fabricated and evaluated as an embedded power device for digital signal, analog signal and power management. The BEOL transistor is three-dimensionally integrated into the metallization layer of the Si-based FEOL device, and is completely isolated from the silicon substrate, resulting in improved noise and interference tolerance. In addition, it has gained significant attention as a possible pathway for increasing IC density and for reducing interconnect delays and ac power consumption by reducing interconnect distances [2]. In particular, a wide band gap semiconductor is advantageous for on-chip bridging I/Os applications embedded in CMOS MCU cores [3].

Therefore, in this study, BEOL transistors were fabricated using oxide semiconductor materials. Since the BEOL transistors are fabricated on the higher level interconnection of devices across the die, integration on BEOL-processed wafers poses a stringent thermal budget with substrate temperatures that need to be <400 °C to prevent damage to the Cu lines and FEOL devices. We applied the IZO film to the active channel layer because of its high mobility and electrical properties in low temperature annealing [4]. In addition, we have fabricated IZO TFT inverters with drain offset channel for high/low converting operation of Si system LSI and stable operation at high voltage drain voltage (V_D). The electrical characteristics of the IZO channel BEOL transistor were measured and the DC and AC operations of the channel offset inverter were evaluated.

2. General Instructions

In this study, a p-type Si substrate with 100-nm-thick thermal SiO_2 was used as the starting material. TiN/Cu/TiN metal layers were continuously deposited in a thickness of 10/100/10 nm and then gate electrodes were formed in a lift-off method. A 10/80-nm-thick Si_3N_4/SiO_2 layer was deposited by RF magnetron sputtering to form the gate insulator of the BEOL transistor. Then, a 50-nm-thick IZO (In:Zn = 1:1 mol%) channel layer was deposited using an RF magnetron sputter, and an active region was formed by photolightograpy and etched with a buffered oxide etchant (BOE) solution. After depositing a 10/100-nm-thick Ti/Al film and forming a S/D electrode by a lift-off method, heat treatment is performed in the forming gas at 350 °C for 30 min.

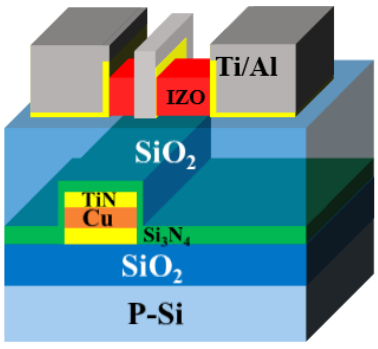

Fig. 1 Schematic structure of fabricated IZO BEOL transistors.

Fig. 1 shows the schematic diagram of fabricated IZO BEOL transistors. The electrical characteristics of the BEOL transistor and the DC inverting of the channel offset invertor were measured with the Agilent 4156B Precision Semiconductor Parameter Analyzer and the AC inverting was meas-

ured with the Agilent 8110A Pulse Generator. All experiments were carried out in a dark room to avoid light and electrical noise.

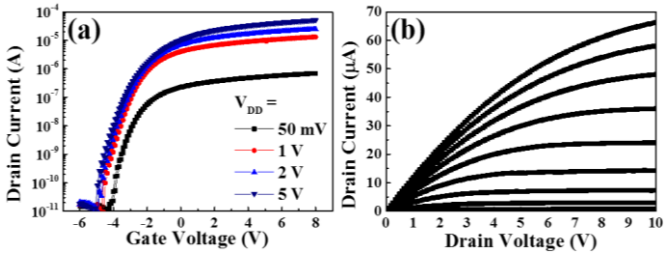

Fig 2. (a) Transfer characteristic (I_D-V_G) curves and (b) Output characteristic (I_D-V_D) curves for IZO BEOL transistors.

Fig. 2 shows the transfer characteristic (I_D-V_G) and output characteristic (I_D-V_D) curves of the BEOL transistor. The channel width (W) and length (L) of the measured BEOL transistors were 30 μm and 50 μm, respectively. The capacitance (C_{ox}) of the Si_3N_4/SiO_2 (10/80 nm) gate insulator was 61.9 pF and the equivalent oxide thickness (EOT) was about 85 nm. It is found that the fabricated IZO BEOL transistor s have n-type transistor operating characteristics, low leakage current, high on/off current ratio and low subthreshold swing (SS). From the transfer characteristic curve of the IZO BEOL transistors, the interface state density (D_{it}) and channel trap density (NSS) can be calculated using Eq. (1) [5]:

$$SS = \frac{qk_BT\left(N_{ss}t_{ch} + D_{it}\right)}{C_i \log(e)} \quad (1)$$

where q, k_B, T, C_i and t_{ch} are the electron charge, Boltzmann's constant, absolute temperature, gate insulator capacitance per unit area, and channel thickness, respectively. It is assumed that D_{it} or N_{SS} are individually set to 0 to extract N_{SS} or D_{it} from the value of SS.

Table I summarizes the electrical parameters of the IZO BEOL transistors. The fabricated IZO BEOL transistors exhibited trap density, high on-off current ratio and high μ_{FE} of 27.36 $cm^2/V{\cdot}s$ even though the annealing temperature is lower than 400 °C.

Table I. Electrical parameters of IZO BEOL transistor at V_D = 1 V.

μ_{FE} [$cm^2/V{\cdot}s$]	SS [V/dec]	D_{it} [$cm^{-2}{\cdot}eV^{-1}$]	N_{ss} [$cm^{-3}{\cdot}eV^{-1}$]	V_{th} [V]	I_{on}/I_{off}
27.4	**0.63**	**2.7×10^{12}**	**5.4×10^{17}**	**-2.1**	**1.4×10^{6}**

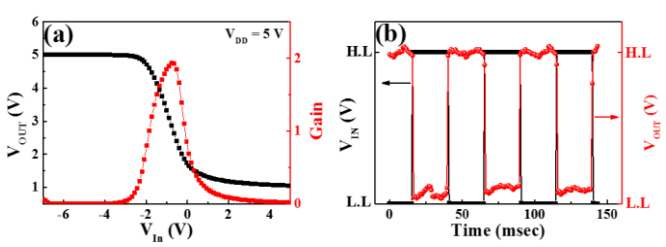

Fig 3. Inverting operation of (a) DC and (b) AC for IZO BEOL TFT inverters with drain offset.

Fig. 3(a) and (b) show the stable inverting operation in DC and AC in an resistor-type inverter with an 80 μm drain offset in the IZO channel. Thus, we conclude that the BEOL transistors with drain offset in the IZO channel is advantageous in implementing high-performance PMICs integrated into 3-D with excellent electrical characteristics and inverting operation.

3. Conclusions

In this study, IZO BEOL transistors were fabricated and their electrical properties were measured. We used TiN/Cu/TiN gate electrode and Si_3N_4/SiO_2 stacked gate insulator. In addition, low-temperature heat treatment at 350 °C was carried out to prevent damage to the lower FEOL Si device level or BEOL interconnect levels. These process conditions enable the creation of more integrated power management ICs in a 3D structure. The fabricated IZO BEOL transistor shows high μ_{FE} of 27.36 $cm^2/V{\cdot}s$ and low D_{it} of 2.68×10^{12} $cm^{-2}{\cdot}eV^{-1}$. Furthermore, the IZO inverters as a fundamental building block of logic circuits were implemented using a drain offset structure and obtained stable inverter characteristics. Thus, BEOL transistors and drain offset structures using IZO metal oxide semiconductors are expected to be promising components for functional logic devices as well as monolithic 3-D integrated PMICs.

Acknowledgements

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