Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp293-294

Recent Topics of Vertical GaN Power Devices - Trench MOS SBDs and Trench MOSFETs -

T. Oka, T. Ina, Y. Ueno, N. Tanaka, J, Kurosaki, T. Suzuki, J. Nishii
K. Hasegawa, K. Yasunishi, G. Nishio, S. Murakami and N. Murakami

TOYODA GOSEI Co., Ltd
1-1, Higashitakasuga, Futatsudera, Ama
Aichi 490-1207, Japan
Phone: +81-52-449-5790 E-mail: toru.oka@toyoda-gosei.co.jp

Abstract

In this paper, recent topics of vertical GaN power devices fabricated on GaN substrates are presented with emphasis on trench MOS SBDs and trench MOSFETs we developed.

1. Introduction

GaN is a promising material for high frequency and high power devices due to its wide band gap, high electron velocity, high breakdown field strength, and high thermal conductivity. In recent years, vertical GaN devices on GaN substrates have attracted considerable attention. The vertical devices have a definite advantage over lateral devices in that the vertical devices increase a blocking voltage by increasing the thickness of the drift region without sacrificing the device size, leading to the implementation of high power density chip. To date, there have been many reports on vertical GaN devices with excellent characteristics such as high blocking voltage or high current p-n junction diodes or Schottky barrier diodes (SBDs) [1-3], junction barrier Schottky (JBS) rectifiers [4,5], trench MOS barrier SBDs [6,7], trench MOSFETs [8-11], HFETs with regrown AlGaN/GaN layers [12,13], and fin power FETs [14,15].

We have reported vertical GaN SBDs and MOSFETs with high blocking voltage, low on-resistance, and high current operations [3,7-10]. In this paper, recent topics of our vertical GaN power devices are presented with emphasis on the trench MOS SBDs and the trench MOSFETs.

2. Trench MOS SBDs

A schematic cross section of the fabricated GaN trench MOS SBD is shown in Fig. 1. The detailed condition of the fabrication was explained elsewhere [7]. The SBD comprises multiple MIS structure trenches covered with insulating films and buried with a wiring electrode. In this structure, the electric field at the Schottky contact can be reduced by extending the depletion region from the sidewalls of the trenches. As a result, a leakage current at reverse bias operation can be suppressed compared to conventional SBDs.

Figure 2 shows the comparison of the reverse *I–V* characteristics of the trench MOS SBD and the conventional SBD designed with having the same forward characteristics. Although the both devices had almost the same V_{on} and R_{on}, the leakage current of the trench MOS SBD was about two orders of magnitude lower than that of the conventional SBD and, as a result, the blocking voltage at a leakage current of 1 mA/cm^2 was increased from 550 V to over 800 V.

Figure 3 shows forward and reverse *I–V* characteristics of the trench MOS SBD chips measured at 25, 100, and 200 °C. The forward current up to 50 A and the blocking voltage over 700 V were achieved even at 200 °C, indicating that the developed trench MOS SBDs are effective for attaining both high-power and high-temperature operations.

3. Trench MOSFETs

A schematic cross section of our developed GaN trench MOSFETs and their details of fabrication were explained elsewhere [8-10]. Here we present switching characteristics and further high current operations of the trench MOSFET chips designed and fabricated with lower chip resistances.

Figure 4 shows the switching waveforms of resistive-load turn-on and turn-off operations for an 80-mΩ MOSFET chip measured at a supply voltage V_{DD} of 300 V and a drain current I_D of 10 A. For comparison, we also measured the waveforms of commercially available SiC MOSFETs with almost the same specification. The GaN MOSFET exhibited superior turn-on and turn-off characteristics to the SiC MOSFETs. The result is attributed to lower capacitances of our GaN MOSFET than those of the compared SiC MOSFETs.

Figure 5 shows the transfer I_D–V_G and output I_D–V_{DS} characteristics of a trench MOSFET chip with the chip resistance of 30 mΩ. The extracted threshold voltage is about 4 V. The drain current reached 50 A at V_{DS} of 1.5 V and V_G of 25 V. To our knowledge, the current is the highest ever reported for vertical GaN transistors on GaN substrates.

4. Conclusions

We have demonstrated the recent progress of our vertical GaN trench MOS SBDs and the trench MOSFETs. The results verify the great potential of the vertical GaN devices for high power applications.

References

[1] H. Ota *et al.*, *Extended Abstracts of the 2017 International Conference on Solid State Devices and Materials* (2017) 671.
[2] I. C. Kizilyalli *et al.*, IEEE Electron Device Lett. **35** (2014) 654.
[3] N. Tanaka *et al.*, Appl. Phys. Express, **8** (2015) 071001.
[4] Y. Zhang *et al.*, IEEE Electron Device Lett. **38** (2017) 1097.

[5] T. Hayashida *et al.*, Jpn. J. Appl. Phys. **57** (2018) 040302.
[6] Y. Zhang *et al.*, *2016 IEEE International Electron Device Meeting* (2016) 252.
[7] K. Hasegawa *et al.*, Appl. Phys. Express, **10** (2017) 121002.
[8] T. Oka *et al.*, Appl. Phys. Express, **7** (2014) 021022.
[9] T. Oka *et al.*, Appl. Phys. Express, **8** (2015) 054101.
[10] T. Oka *et al.*, *Proc. of the 28th IEEE International Symposium on Power Semiconductor Devices and ICs* (2016) 459.
[11] D. Ji *et al.*, *2017 IEEE International Electron Device Meeting* (2017) 223.
[12] H. Nie *et al.*, IEEE Electron Device Lett. **35** (2014) 939.
[13] D. Shibata *et al.*, *2016 IEEE International Electron Device Meeting* (2016) 248.
[14] M. Sun *et al.*, IEEE Electron Device Lett. **38** (2017) 509.
[15] Y. Zhang *et al.*, *2017 IEEE International Electron Device Meeting* (2017) 215.

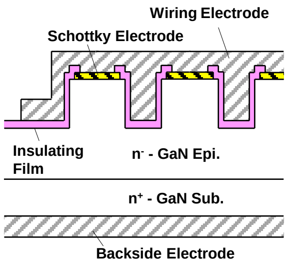

Fig. 1 Schematic cross section of the fabricated trench MOS SBD.

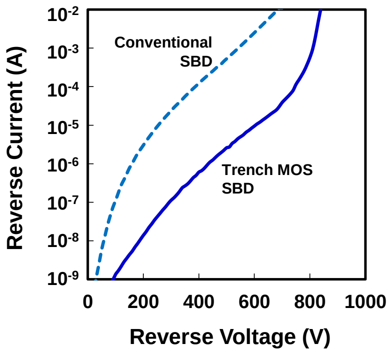

Fig. 2 Comparison of the reverse *I*–*V* characteristics of a trench MOS SBD and a conventional SBD.

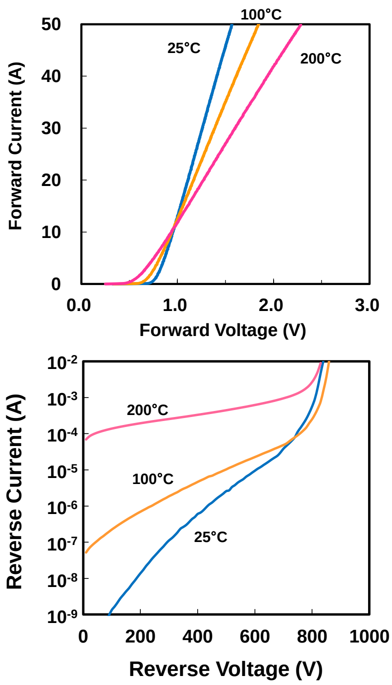

Fig. 3 Forward and reverse *I*–*V* characteristics of the fabricated trench MOS SBD chips measured at 25, 100, and 200 °C.

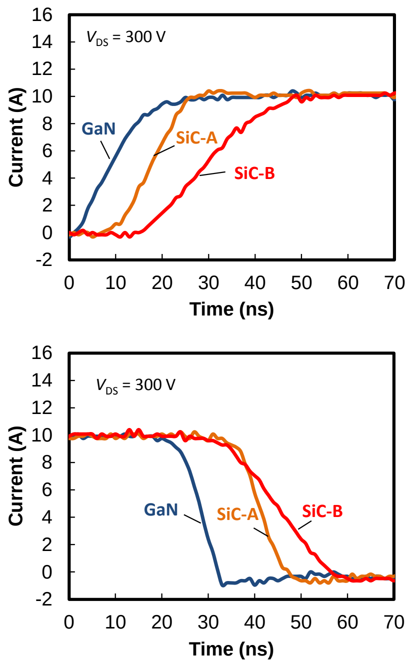

Fig. 4 Switching waveforms of resistive-load turn-on and turn-off operations for an 80-mΩ MOSFET chip.

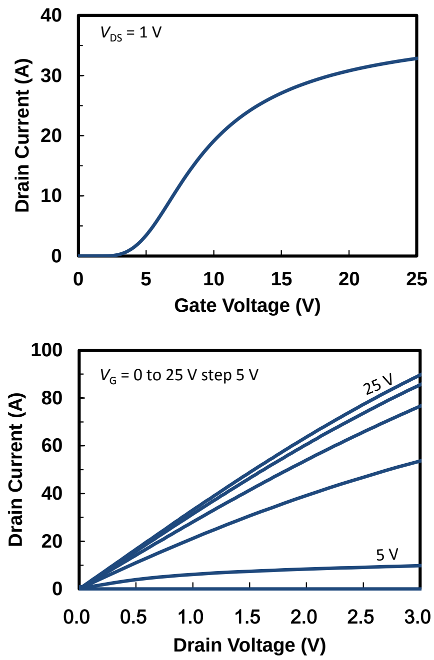

Fig. 5 Transfer I_D–V_G and output I_D–V_{DS} characteristics of a trench MOSFET chip with the chip resistance of 30 mΩ.