

# 100V to 1800V High Performance p-GaN HEMT Epitaxial Layers and E-mode Power Devices on 8-inch Commercial QST® Substrates

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## Abstract

The CMOS fab friendly 8-inch QST® (Qromis Substrate Technology) substrates enable fabrication of commercial high-performance GaN power devices with breakdown voltages ranging from 100V to 1800V. This is achieved by utilizing a substrate core with the coefficient of thermal expansion (CTE) matched to GaN over a wide temperature range [1-3]. In this paper, we announce high-quality and high-breakdown voltage p-GaN HEMT epitaxial layers on revolutionary and CMOS fab friendly 8-inch QST® substrates. Voltage blocking capability up to 1800V is demonstrated by using a 15  $\mu\text{m}$  thick buffer. Further, we present high-performance normally-off p-GaN HEMT transistors with  $V_{th}$  of 2.8V, fabricated on 8-inch QST® substrates in a CMOS fab.

## 1. Introduction

Recent improvements in GaN HEMT device performance and reliability have resulted in a number of commercially available GaN transistors with the breakdown voltage in the range of 100V to 650V. As of today, the existing commercial solutions utilize 6-inch GaN-on-Si technology, which has limited scale capability due to fundamental CTE mismatch challenges of GaN-on-Si epitaxial growth, resulting in highly stressed and/or cracked epitaxial layers or wafer breakage even with thick Si substrates. In this work, we present our recent GaN epitaxy and GaN e-mode power device results on commercially available and patented 8-inch diameter SEMI spec QST® substrates, which enable unique and unmatched scaling advantages in performance, cost, and application for GaN power and RF devices.

## 2. Experimental

The image and construction of the commercial 8-inch QST® substrates that were utilized in this study are shown in Figure 1. As can be seen, the QST® substrate consists of a core material (750  $\mu\text{m}$  thick) wrapped with a series of engineered layers yielding CMOS fabrication line compatibility with SEMI specs. Thin Si (111) layer is formed on top of engineered layers providing single crystal growth surface for GaN epitaxy. The SEMI spec QST® substrate is engineered to achieve low-bow and low-stress state after GaN epitaxy is grown. Due to CTE-matched nature of the QST® substrates, GaN epitaxial layers with thicknesses ranging from a few microns to tens of microns are realized without excessive stress and/or cracking issues. As an evidence, recent results from

independent research groups confirm that several hundred microns thick GaN growth, ultimately yielding free-standing GaN substrates, could be realized on QST® substrates [4].

The GaN HEMT epitaxy results reported here were performed in a commercial MOCVD reactor. The structures of the epitaxial layers used in this study are shown in Figure 2. After growing the AlN/AlGaIn transition layers, the insulating buffer layers (with the thickness range between 2.5 and 15  $\mu\text{m}$ ) were deposited in order to achieve blocking voltages up to 1800V. Finally, standard p-GaN HEMT epitaxial layers were deposited on top of the insulating buffers.

The GaN-on-QST® HEMT epi wafers are tightly controlled for wafer shape with bow of <50  $\mu\text{m}$  which is critical to enable high-yielding device process integration in a conventional CMOS fab.

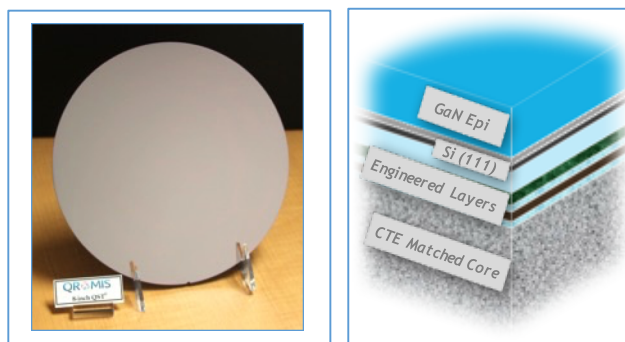


Fig. 1 The image and cross-section of 8-inch QST® substrate.

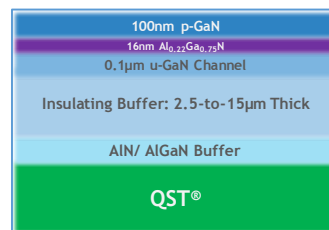


Fig. 2 The structure of the p-GaN HEMT epitaxial layers.

The typical 2DEG values measured on 1200V HEMT structure are shown in Table 1 representing state-of-art parameters for p-gate e-mode devices.

Parameter	Value
Sheet Resistance (ohm/sq)	520
Mobility ( $\text{cm}^2/\text{Vs}$ )	1600
Carrier Concentration ( $\text{cm}^{-2}$ )	7.5E12
Vertical Breakdown @ 1 $\mu\text{A}/\text{mm}^2$	1220

Table 1. 2DEG and breakdown parameters for 1200V HEMT wafer.

The vertical voltage handling capability of the HEMT epitaxial layers with different buffer layer thicknesses were evaluated by I-V tests using evaporated metal contacts on GaN surface and Si (111) growth interface layer. Figure 3 shows the measured I-V characteristics for 6.5 and 15  $\mu\text{m}$  thick buffers. As can be seen, by using a commonly accepted

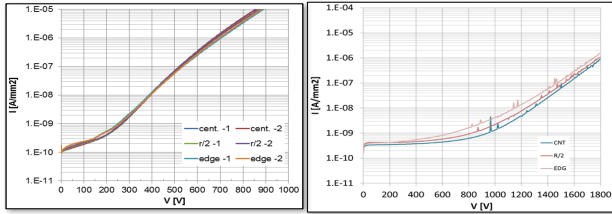


Fig. 3 Vertical leakage tests demonstrating a) 700V and b) 1800V HEMT buffer blocking voltage.

$1\mu\text{A}/\text{mm}^2$  vertical current density limit, the wafers exhibit 700V and 1800V voltage blocking capability, respectively, with high center to edge uniformity. The results for a wide range of buffer thicknesses are summarized in Table 2.

Buffer Thickness ( $\mu\text{m}$ )	Blocking Voltage (V) @ $1\mu\text{A}/\text{mm}^2$
2.5	220
6.5	700
12	1220
15	1800

Table 2. Blocking voltage vs. buffer thickness on 8-inch QST<sup>®</sup>

In order to demonstrate the fundamental capabilities of the GaN-on-QST<sup>®</sup> HEMT epitaxy for device applications, the initial 200V rated p-GaN gate e-mode HEMT devices were fabricated on 8-inch diameter QST<sup>®</sup> wafers in IMEC's CMOS fab (Figure 4). Figure 5 shows the output and the transfer curves for such devices. Figure 6 represents the leakage characteristics of the devices and the buffer. From the results, it can be seen that these devices yield state-of-art characteristics, with  $V_{\text{th}}$  of 2.8V among the best in class.

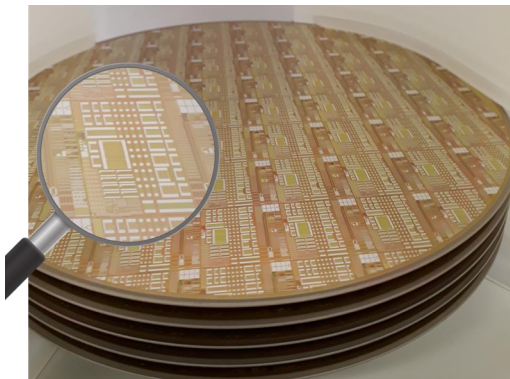


Fig. 4 The image of fully integrated 8-inch e-mode p-GaN HEMT device wafers on QST<sup>®</sup>.

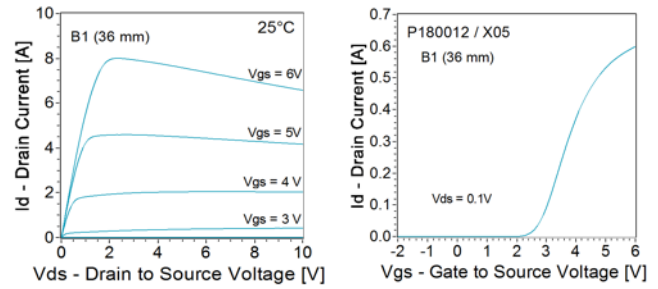


Fig. 5 The output and the transfer curves for 36 mm gate width e-mode devices on 8-inch QST<sup>®</sup> substrates.

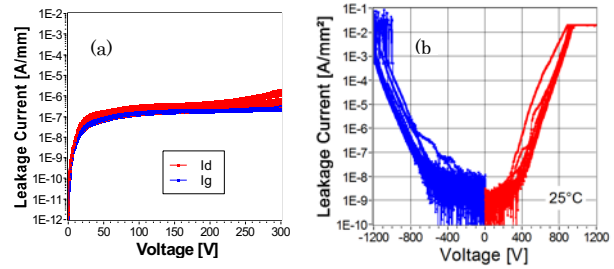


Fig. 6 The leakage data measured across a device wafer: (a) drain and gate leakage, and (b) vertical buffer leakage.

### 3. Conclusions

This paper presents the latest HEMT epi and device results on 8-inch diameter commercial QST<sup>®</sup> substrates with state-of-art device performance and scalability to 1800V blocking voltage.

### Acknowledgements

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