

Investigation of the Si₃N₄/(Al)GaN interface properties in LPCVD Si₃N₄/Al-GaN/GaN MIS-HEMT with Post Deposition Annealing

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Abstract

The influence of the post deposition annealing (PGA) on Si₃N₄/(Al)GaN interface properties in LPCVD Si₃N₄/AlGaN/GaN MIS-HEMT was investigated by *IV* and *CV* measurement. With high temperature annealing at 650 °C and O₂ ambient, the gate leakage was reduced almost 1 order, from 10⁻⁷ mA/mm to 10⁻⁸ mA/mm, thus, an enhanced *I*_{ON}/*I*_{OFF} ratio from 10⁹ to 10¹⁰. The *CV* results showed an optimized Si₃N₄/(Al)GaN interface with the trap density of 10¹¹ cm⁻²eV⁻¹ after annealing. The ON-resistance (*R*_{ON}) degradation was only 33% at 600 V quiescent drain bias, indicating excellent interface properties at the active region because of the PGA process.

1. Introduction

GaN-based power devices are expected to compete with Si-based power devices in low energy consumption and high-efficiency power systems, owing to their superior material properties [1]. Especially, AlGaN/GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) demonstrated with low leakage, high *I*_{ON}/*I*_{OFF} ratio and large forward gate voltage swing are promising candidates to outperform Si-based devices for applications below 600 V [2]. Among the types of dielectric materials, Si₃N₄ dielectric films deposited at high temperature (e.g., 780 °C) using low pressure chemical vapor deposition (LPCVD) has shown superior performance in terms of low leakage, high-breakdown electric field, and long time-dependent-dielectric-breakdown (TDDDB) lifetime [2]. For recent years, LPCVD Si₃N₄ used as passivation layer was also proposed and studied to suppress the current collapse in active area [2]. Though lots of technology have been proposed to deal with the SiN/(Al)GaN interface to improve the devices performance and reliability, the properties of the SiN/(Al)GaN interface still far from expected.

In this work, we proposed an early SiN deposition process, in which the SiN film served as gate dielectric and passivation layer. With the special annealing process in O₂ ambient at 650 °C, the SiN/(Al)GaN interface was improved a lot. The trap density (*D*_{it}) is below 10¹² cm⁻²eV⁻¹ and the dynamic *R*_{ON} is only 1.33 times over the static one.

2. Experiment and results

The AlGaN/GaN heterostructure used in this work was

grown by the metal organic chemical vapor deposition (MOCVD). The reported devices were fabricated in a 6-inch silicon foundry. The commercial AlGaN/GaN epilayer consisted of a 4-μm GaN buffer layer, a 300-nm GaN channel layer, a 25-nm Al_{0.25}Ga_{0.75}N barrier layer and a 2-nm GaN cap layer for improved surface morphology. On wafer Hall measurement yields a sheet resistance of 360 Ω/square, a 2DEG density of 1×10¹³ cm⁻², and an electron mobility of 1500 cm²/V·s.

The process started with the mesa etching, followed by the deposition of a 30-nm thick Si₃N₄ layer on the heterostructure using LPCVD. After which, the wafer was annealed in O₂ ambient at 650 °C for 10 min. Then, a 500-nm SiO₂ layer was deposited by PECVD, which was used for passivation and planarization. Ti/Al/Ti/TiN based ohmic contact was formed after recessing the SiO₂ passivation layer, Si₃N₄ layer and the AlGaN barrier layer successively. Then, the gate foots were defined by a combination of SF₆ low power ICP etching and BOE wet etching. Finally, the TiN/Ti/Al gate metal was deposited by physical vapor deposition (PVD) method and patterned by dry etching. For comparison, the device without annealing was also fabricated on the same heterostructure at the same time. The both devices under studied feature same dimension of *L*_G/*L*_{GS}/*L*_{GD}/*W*=1.5/5/20/250 μm.

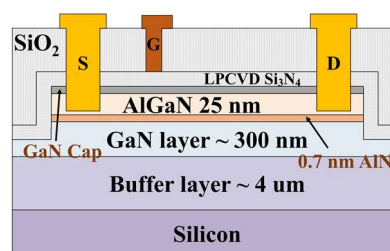


Fig. 1 Cross-section of the fabricated MIS-HEMT device.

Fig. 2 (a) and (b) shows the *IV* characteristics of the MIS-HEMTs with and without PGA process, respectively. The *R*_{ON} are similar for the devices with the value of 10.75 Ω·mm and 11.61 Ω·mm. The maximum current is both above 700 mA/mm, with slightly higher in the PGA MIS-HEMT. Fig. 3 compares the transfer performance of the MIS-HEMTs. It is clear that the PGA MIS-HEMT deliver almost 1 order

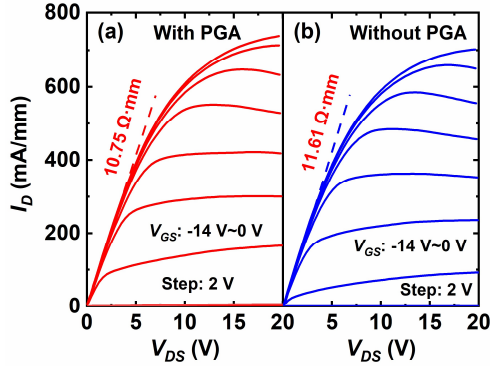


Fig. 2 I_V curves of the MIS-HEMT (a)with and (b)without PGA.

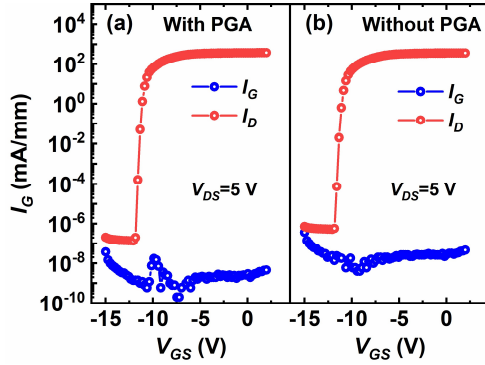


Fig. 3 Transfer curves of the MIS-HEMT (a)with and (b)without PGA.

lower gate leakage current, resulting in 1 order increase in I_{ON}/I_{OFF} ratio from 10^9 to 10^{10} . This indicates an improved Si_3N_4 film was obtained because of the PGA.

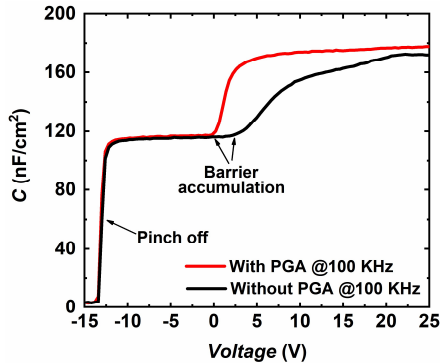


Fig. 4 CV curves of the MIS-HEMT with and without PGA.

Fig. 4 shows the CV data of the MIS-HEMTs. The Si_3N_4 depletion voltage is much high in the MIS-HEMT without PGA, which means high D_{it} in the Si_3N_4 or $\text{Si}_3\text{N}_4/(\text{Al})\text{GaN}$ interface [3]. The frequency-dependent conductance method was used to extract D_{it} . The D_{it} is in order of $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ for PGA interface, which is almost 2 orders lower than that in the none PGA device. This may be explained as the fix charge in the Si_3N_4 or $\text{Si}_3\text{N}_4/(\text{Al})\text{GaN}$ interface was compensated by O^2 . Fig. 5 shows the pulsed I_D - V_{DS} measurement under fast switching with different quiescent bias points (V_{GS0} , V_{DS0}). The pulse width is $10 \mu\text{s}$ and the period is 1 ms . It can be seen that the degradation of dynamic on-resistance is only 33% at 600 V quiescent bias for PGA MIS-HEMT, which is smaller

than the previous report with $\text{AlN}/\text{Si}_3\text{N}_4$ passivation [4].

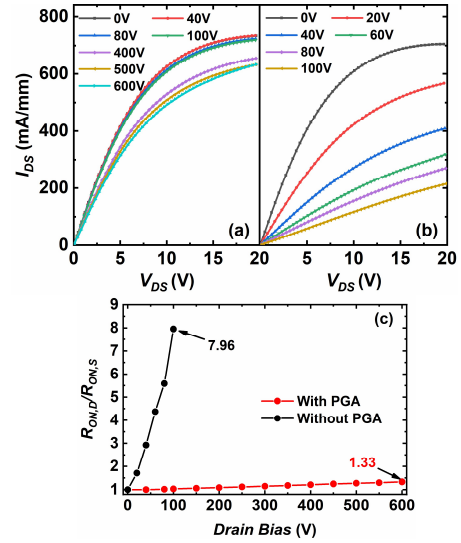


Fig. 5 Pulsed I_V output of the device (a)with and (b) without PGA under different quiescent biases ($V_{GS}=2 \text{ V}$). (c) Ratio of the dynamic on-resistance over the static one ($R_{ON,D}/R_{ON,S}$) of the fabricated MIS-HEMTs at different quiescent drain bias points.

3. Conclusions

In this work, the influence of the PGA on $\text{Si}_3\text{N}_4/(\text{Al})\text{GaN}$ interface properties in LPCVD $\text{Si}_3\text{N}_4/\text{AlGaIn}/\text{GaIn}$ MIS-HEMT was studied. The LPCVD grown Si_3N_4 served as gate dielectric as well as the passivation layer. Therefore, with the PGA process, the gate reliability and dynamic RON performance are all optimized. Further investigation will be done to clarified the mechanism of the PGA influences in the LPCVD $\text{Si}_3\text{N}_4/\text{AlGaIn}/\text{GaIn}$ MIS-HEMT.

Acknowledgements

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