A Superior 15–kV SiC MOSFET with Current Spreading Layer for High–Frequency Applications

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Abstract
A superior 15–kV silicon carbide (SiC) metal–oxide–semiconductor field–effect transistor (MOSFET) with a current spreading layer (CSL) implanted by nitrogen ions has been developed for high–frequency applications. The CSL and junction field–effect transistor (JFET) region were optimized via device simulation to reduce the on–resistance. A SiC MOSFET with a CSL and a die size of 5 mm × 5 mm was fabricated. The specific on–resistance was estimated to be 191 mΩ·cm². The blocking voltage of 15.0 kV was obtained. Owing to the narrow JFET width of 0.8 µm, the reverse transfer capacitance was 0.6 pF at 6 kV. In addition, a threshold voltage shift within ± 0.1 V was achieved at a gate voltage of −15 V and at 200 °C for 1000 h.

1. Introduction
Silicon carbide (SiC) power devices with a blocking voltage ($V_b$) greater than 10 kV are required for the power supplies of electron guns, high–power medium–voltage converters [1], and narrow pulse applications [2]. SiC metal–oxide–semiconductor field–effect transistors (MOSFETs) are suitable for high–frequency applications in comparison with SiC insulated–gate bipolar transistors (IGBTs) [3]. The reverse transfer capacitance ($C_{rrx}$) must be reduced for high–frequency and highly efficient switching power supplies [4]. However, there is a trade–off relation between on–resistance ($R_{on}$) and $C_{rrx}$. Moreover, junction field–effect transistor (JFET) regions result in a high $R_{on}$ because a high–voltage (>10 kV) SiC MOSFET is composed of a $n^-$ drift region with a low doping concentration. In the authors’ previous work [5], the JFET region of a 13–kV SiC MOSFET without a current spreading layer (CSL) was intentionally optimized to simultaneously achieve a high $V_b$ and low specific on–resistance ($R_{on, sq}$). In this work, a sufficiently reliable 15–kV SiC MOSFET with a CSL was developed to reduce $C_{rrx}$ without increasing the $R_{on}$.

2. Device Design and Fabrication
Figure 1 shows a cross–sectional structure of the unit cell of 15–kV SiC MOSFETs without and with a CSL. First, the characteristic with the CSL and JFET regions was optimized. A two–dimensional Sentaurus device simulator (Synopsys Inc., technology computer–aided design) was used to evaluate the relation between the $R_{on, sq}$ and the $V_b$.

![Cross-sectional schematics of SiC MOSFETs (a) without and (b) with a CSL.](image)

Fig. 1 Cross–sectional schematics of SiC MOSFETs (a) without and (b) with a CSL.

3–1. Dependencies of $R_{on, sq}$ and $V_b$ on the JFET width
Figure 2 shows the simulation and experimental results for SiC MOSFETs without and with a CSL for $R_{on, sq}$ as functions of JFET width. These results indicate that $R_{on, sq}$ of the SiC MOSFETs without a CSL depends on the JFET width. As the JFET width decreases at less than 1.6 µm, $R_{on, sq}$ of the SiC MOSFETs without a CSL abruptly increases. This is due to the current crowding phenomenon at the top of the drift region because the depletion layer spreads from the $p$–base region. In contrast, $R_{on, sq}$ of the SiC MOSFETs with a CSL is roughly constant with respect to the JFET width from 0.6 µm to 1.8 µm. The CSL relays the concentration of the current distribution at the top of the drift region.

![Simulation (open marks) and experimental results (closed marks) of SiC MOSFETs with and without a CSL.](image)

Fig. 2 Simulation (open marks) and experimental results (closed marks) of SiC MOSFETs with and without a CSL.
Figure 3 shows comparison between the simulation and experimental results for SiC MOSFETs with a CSL. These results indicate that the $V_{th}$ is roughly constant with respect to the JFET width. $R_{on,eq}$ of the SiC MOSFET with a CSL is also roughly constant in the range of JFET widths of 0.8–1.6 µm. The experimental results are in good agreement with the simulation results.

Fig. 3 Relation between $R_{on,eq}$ and $V_{th}$ on the SiC MOSFETs with various JFET widths. The open and the closed marks show the simulation and the experimental results, respectively.

3–2. Electrical Properties of 15–kV MOSFETs

Figures 4 and 5 show the $I–V$ characteristics and $V_{th}$ of a SiC MOSFET with a size of 5 mm × 5 mm, respectively. $R_{on,eq}$ was estimated to be 191 mΩ·cm² at 25°C. The $V_{th}$ of 15.0 kV was obtained at 1 µA at room temperature.

Fig. 4 $I_{DS}$–$V_{DS}$ characteristics of a SiC MOSFET with a size of 5 mm × 5 mm at 25°C (solid line) and 150°C (dashed line). (measured on a wafer)

Fig. 5 $V_{th}$ of a SiC MOSFET with a size of 5 mm × 5 mm at room temperature (measured on a wafer).

Figure 6 shows the dependencies of $C_{rss}$ and $R_{on}$ on the JFET width. As the JFET width decreases, $C_{rss}$ decreases, and $R_{on}$ is almost constant. The figure of merits defined as $R_{on} \times C_{rss}$ is an indicator for high–frequency applications. Therefore, a SiC MOSFET with the narrow JFET width is superior for high–frequency applications.

Fig. 6 Dependencies of the $C_{rss}$ and $R_{on}$ on the JFET width. The $C_{rss}$ was measured at gate–drain voltage of 6 kV.

3–3. Reliability

Figure 7 shows the threshold voltage ($V_{th}$) shift of 15–kV MOSFETs for elucidating the long–term reliability of the gate oxide. When applying a gate voltage of −15 V, which is equal to the gate–oxide electric field of −3MV/cm, a $V_{th}$ shift within ±0.10 V is obtained from 1 h until 1000 h at 200 °C. A small $V_{th}$ shift is significant for preventing series–connected or parallel–connected SiC MOSFETs from falsely turning on and turning off.

Fig. 7 Threshold voltage shift under bias stress instability test at 200°C.

4. Conclusions

Owing to the use of a device simulator, the fabricated 15–kV SiC MOSFET simultaneously achieves a high $V_{th}$, low $R_{on,eq}$ and low $C_{rss}$. Therefore, the 15–kV SiC MOSFET with the CSL is superior for high–frequency applications.

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References