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Double RESURF JTEs Structure for Low On-Resistance Trench Gate SiC MOSFET

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Abstract

We have developed V-groove trench gate SiC MOSFETs (VMOSFETs) with double reduced surface field junction termination extensions structure (DR-JTEs). Simulation results showed that the DR-JTEs has a breakdown voltage that corresponds to 94% of the ideal 1D parallel plane value. The VMOSFETs with the DR-JTEs structure demonstrated both a breakdown voltage of 1610 V and specific on-resistance of 2.4 mΩcm^2.

1. Introduction

Wide band-gap semiconductors based on silicon carbide (SiC) are most attractive for high power devices due to low losses, improved temperature capability and high thermal conductivity. Developments of low specific on-resistance SiC MOSFETs have been pushed forward for expanding applications at a medium voltage region (600-1700 V) including power supplies and electric/hybrid vehicles [1].

Minimizing the surface area of trench gate MOSFETs is effective in lowering the specific on-resistance. On the other hand, this design method for trench gate MOSFETs with a p-type region at the bottom of trench, has limitations of increasing the resistance of a JFET structure between the bottom end of a p-well region and the p-type trench bottom region in a smaller unit cell. To alleviate this problem, a heavily doped n-type current spreading layer (CSL) below the p-well regions at a certain depth is well applied to the top of the drift layer by epitaxial re-growth [1].

However, a higher n-type doping density in the surface layer impedes lateral expansion of the depletion region from the p-n junction at an edge-termination structure that includes junction termination extensions (JTEs) and floating field-ring terminations [1], which leads to a poor breakdown voltage of the MOSFETs far from the ideal value. Therefore, practical JTE structures for the heavily doped n-type surface layer are necessary for developing low specific on-resistance MOSFETs.

In this paper, the authors have designed a double reduced surface field (RESURF) JTEs structure (DR-JTEs) applicable for the heavily doped n-type surface layer and fabricated 1.2 kV-class SiC trench MOSFETs with an optimized JTE dose.

2. Device structure

2.1. SiC VMOSFET

V-groove trench gate SiC MOSFETs (VMOSFETs) with the 4H-SiC$\{0\bar{3}3\bar{8}\}$ face trench sidewalls have demonstrated low specific on-resistance and excellent stability in threshold voltage owing to a low interface trap density of SiO_2/SiC [2, 3]. Figure 1 shows the 1.2 kV-class VMOSFETs that has the buried p^+ regions under the trench bottom and the p^+ source regions. The buried p^+ regions protect the gate oxide from a high electric field breakdown in the off-state. Lateral and vertical JFET structures exist between the bottom end of the p-well region and the buried p^+ regions. An n-type ion implantation was applied to the vertical JFET region and an epitaxial surface re-growth layer with a heavy n-type doping was incorporated in the lateral JFET region in order to reduce the parasitic resistance.

2.2. JTE structures

Figure 2 shows the schematic cross section of the proposed SiC VMOSFETs with the DR-JTEs and conventional two-zone JTE (TZ-JTE) structure. The device structure consists of a 350 μm thick n^+ SiC substrate, an n-drift layer with thickness of 11.5 μm and doping concentration of 8×10^{15} cm^{-3}, an n^+ surface re-growth layer with thickness of 1 μm and doping concentration of 5×10^{16} cm^{-3}, buried p^+ regions, and a p^{++} source contact region. The DR-JTEs features both the JTE1 formed in the n^+ surface re-growth layer surrounded by the floating rings and the JTE2 buried in the n-drift layer. The width of the edge termination region of these devices is 45 μm.

Figure 3 exhibits the simulated JTE1 dose dependence of the breakdown voltage of the DR-JTEs by Sentaurus of Synopsis™ TCAD. The proposed DR-JTEs reduces the sensitivity of the breakdown voltage over the JTE dose. These simulation results indicate a wide optimum JTE dose window as for a breakdown voltage of over 1620 V of the simulated VMOSFETs. The simulated breakdown voltage of the DR-JTEs structure at a JTE1 dose of 1.4×10^{13} cm^{-2} is 1690 V. This value corresponds to 94% of the ideal parallel-plane breakdown voltage estimated from 1D simulation of p-n junction of the doping concentration and the epitaxial layer thickness without the CSL.

The electric field distributions at breakdown voltage in the DR-JTEs with various JTE1 doses are shown in Fig. 4. An electric field crowding takes place at the edge of the buried p^+ regions in the case of a lower JTE1 dose (0.5×10^{13} cm^{-2}). The breakdown point moves from the buried p^+ regions

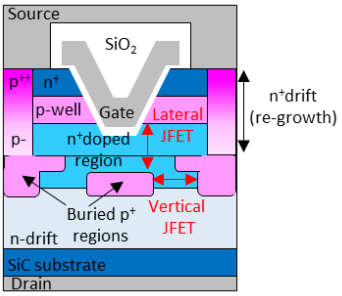

Fig. 1 Schematic view of the intersection cell structure of VMOSFET.

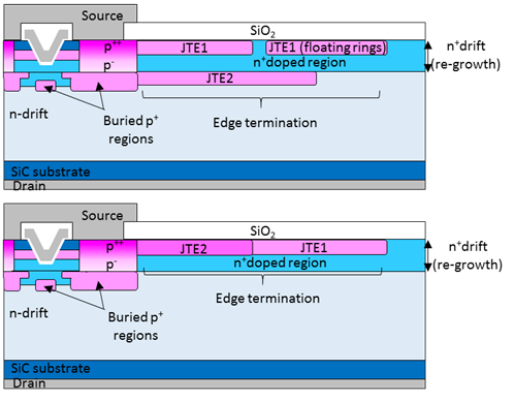

Fig. 2 Schematic cross section of the SiC VMOSFET with the DR-JTEs (upper) and conventional TZ-JTE (lower).

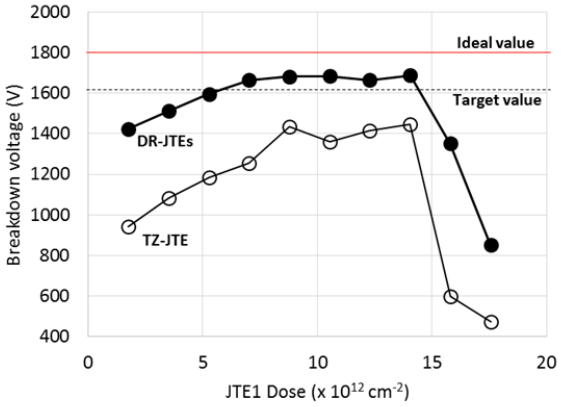

Fig. 3 JTE1 dose dependence of simulated breakdown voltage for the DR-JTEs and the TZ-JTE.

to the JTE2 with a dose of 1.1×10^{13} cm^{-2}. In the case of a higher dose (1.6×10^{13} cm^{-2}), breakdown occurs at the outer ring in the n$^+$ surface re-growth layer. This result indicates that the DR-JTEs at off-state effectively depletes the n$^+$ surface re-growth layer and suppresses electric-field-crowding at the edge of p-n junction in the surface layer.

3. Results and discussion

Figure 5 shows typical blocking characteristics and the forward I_D–V_{DS} curve of the fabricated VMOSFETs with the DR-JTEs at the JTE1 dose of 8.8×10^{12} cm^{-2}. It is found that a breakdown voltage is 1610 V and is almost comparable to the simulated breakdown voltage of the VMOSFETs. In addition, the proposed device with an active area of 0.0377 cm^2

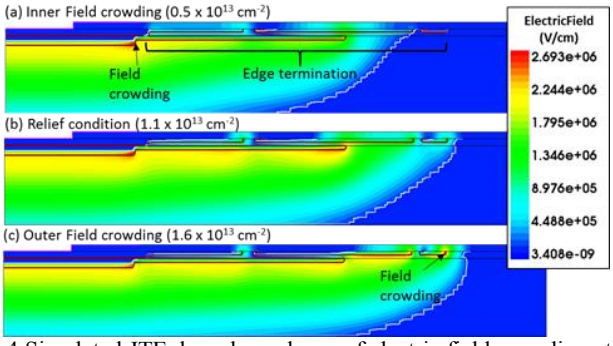

Fig. 4 Simulated JTE dose dependence of electric field crowding at breakdown voltage in edge termination region.

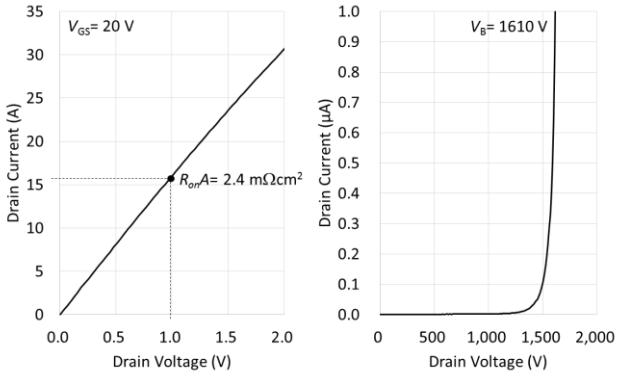

Fig. 5 Typical blocking characteristics and forward I_D–V_{DS} curve of fabricated VMOSFETs with the DR-JTEs.

exhibits a low specific on-resistance of 2.4 mΩcm^2 (including a substrate resistance of 0.7 mΩcm^2) at room temperature. A threshold voltage of the device is 5.1 V, which is defined as a gate voltage of a drain current of 0.1 mA at a drain voltage of 10 V.

4. Conclusions

In this paper, the double RESURF JTEs (DR-JTEs) structure for low specific on-resistance SiC MOSFETs with wide JTE dose tolerance was proposed.

The simulated breakdown voltage of the DR-JTEs at an optimum JTE dose was 94% of the ideal parallel-plane breakdown voltage. The 1.2 kV SiC VMOSFETs with the proposed JTE structure demonstrated both a high breakdown voltage of 1610 V and a low specific on-resistance of 2.4 mΩcm^2 with a threshold voltage of 5.1 V. These results indicate that the SiC VMOSFETs with the DR-JTEs are promising devices for medium voltage applications.

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