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# Impact of $Al_2O_3$ interlayer for metal-oxide-semiconductor capacitor on (111) oriented 3C-SiC for electronic device application

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**Abstract**

**MOS capacitors with various interlayer (IL) were fabricated on (111) oriented n-type 3C-SiC. Sputter deposited $SiO_2$ without IL and thermally grown $SiO_2$ show deteriorated *C-V* characteristics. By inserting IL, *C-V* characteristics are significantly improved. Especially, ALD $Al_2O_3$-IL is suitable for 3C-SiC, which successfully achieved low $D_{it}$ on the order of $10^{10}$ $cm^{-2}eV^{-1}$.**

## 1. Introduction

Silicon carbide (SiC) has been attracting much interest as a material for high efficient and small size power devices due to its high breakdown field. It can be apply not only for power device application, but also semiconductor devices which can operate at high temperature environment owing to its wide bandgap. Among some polytypes of SiC, (111) oriented 3C-SiC can be grown on Si (111) surface [1]. Therefore, 3C-SiC/Si hetero-epitaxial substrate has a potential for on-chip hetero-integrated electronic device. In order to apply high feasibility of 3C-SiC for electronic devices, it is necessary to form good insulator on 3C-SiC with high interfacial quality for MOS gate and surface passivation layer. However, conventional thermally oxidized $SiO_2$ on 3C-SiC showed deteriorated characteristics and large negative shift of flat band voltage [2]. As an improvement method for interfacial quality, it is well known that insertion of suitable interlayer (IL) between insulator and semiconductor [3-5]. In this study, we fabricated 3C-SiC MOS capacitors with some kinds of IL. As a results, atomic layer deposited (ALD) $Al_2O_3$-IL is effective to achieve good MOS characteristics with low interface state density ($D_{it}$).

## 2. Experimental

The substrate used in this study was (111) oriented n-type 3C-SiC epitaxially grown on n-Si (111) substrate. Donor (nitrogen) concentration of 3C-SiC is on the order of $10^{16}$ $cm^{-3}$. In this study, we fabricated lateral MOS capacitor [6]. Sample fabrication procedure and cross sectional image are summarized in Fig. 1. After substrate RCA cleaning and dilute HF treatment, an IL was formed by electron cyclotron resonance (ECR) plasma oxidation or ALD $Al_2O_3$ deposition. Then, $SiO_2$ (23-25 nm) was deposited as a gate insulator by using ECR plasma sputtering. Next, post deposition annealing (PDA) was performed at 400-600°C in $N_2$ ambient. Al electrode was formed by thermal evaporation, and it was patterned standard lithography and wet etching techniques for gate and contact electrodes. For a comparison, MOS capacitors without IL and thermally oxidized $SiO_2$ insulator were also fabricated. Details of all samples are summarized in Table I. Capacitance-Voltage (*C-V*) measurement with frequency range of 1 M – 100 Hz was carried out and $D_{it}$ was evaluated by using Hi-Low frequency method [7].

## 3. Result and Discussion

Figure 2 shows high frequency (500 k or 100 kHz) *C-V* characteristics for some samples. Typical n-type *C-V* curves were obtained for all samples, which means crystal quality of the 3C-SiC is good. However, there are large differences among MOS fabrication methods. "#1 no-IL" shows stretch-outed *C-V* curve which originates from large amount of $D_{it}$. *C-V* curves are improved by IL insertion as shown "#2 plasma oxidized-IL" and "#4 $Al_2O_3$-IL (PDA 500°C)". Particularly, "#4" shows very sharp *C-V* curve. Sample with thermally oxidized $SiO_2$ "#6" shows large negative shift which suggests there are large amount of positive fixed charge in $SiO_2$ and it relates C atom in $SiO_2$ [2].

Figure 3 shows *C-V* hysteresis for $Al_2O_3$-IL samples "#3-5" with different PDA temperatures. *C-V* curve shifts to negative direction as PDA temperature increases. Hysteresises are negligible for all SiC samples. Namely, $Al_2O_3$-IL well suppressed carrier injection to gate insulator from 3C-SiC substrate. Interestingly, n-Si MOS with the same gate structure shows large clockwise hysteresis. In order to clarify the reason of this difference, further study is needed.

*C-V* frequency dependences for some samples are shown in Fig. 4. "#1 no-IL" and "#6 thermally oxidized $SiO_2$" have large frequency dispersion at depletion state. On the other hand, IL inserted samples ("#2" and "#4") suppressed frequency dispersion. $D_{it}$ distribution for all samples are summarized in Fig. 5. $Al_2O_3$-IL is effective to reduce $D_{it}$. Especially, "#4 PDA 500°C" achieved very low $D_{it}$ on the order of $10^{10}$ $cm^{-2}eV^{-1}$ at upper-half of energy bandgap.

## 3. Conclusions

We fabricated MOS capacitor on (111) n-type 3C-SiC. IL insertion is effective to improve *C-V* characteristics. MOS capacitor with ALD $Al_2O_3$-IL shows very sharp *C-V* curve and extremely low $D_{it}$. ALD $Al_2O_3$ has a potential as gate IL and passivation layer for 3C-SiC device application.

| No. | Insulator | Interlayer(IL) | PDA temp. (°C) | EOT (nm) | Flat band voltage (V) |
|---|---|---|---|---|---|
| #1 | Sputter deposited $SiO_2$ (23-25 nm) | Nothing | 400 | 24.7 | 0.27 |
| #2 | | ECR plasma oxidation | 400 | 25.3 | 0.56 |
| #3 | | ALD $Al_2O_3$ (5 nm) | 400 | 24.0 | -0.37 |
| #4 | | | 500 | 23.9 | -0.78 |
| #5 | | | 600 | 24.3 | -1.13 |
| #6 | Thermally grown $SiO_2$ (1200°C) | | | 18.8 | -4.53 |

Table I Details of the fabricated MOS capacitors on 3C-SiC. Equivalent oxide thickness (EOT) and flat band voltage are also listed.

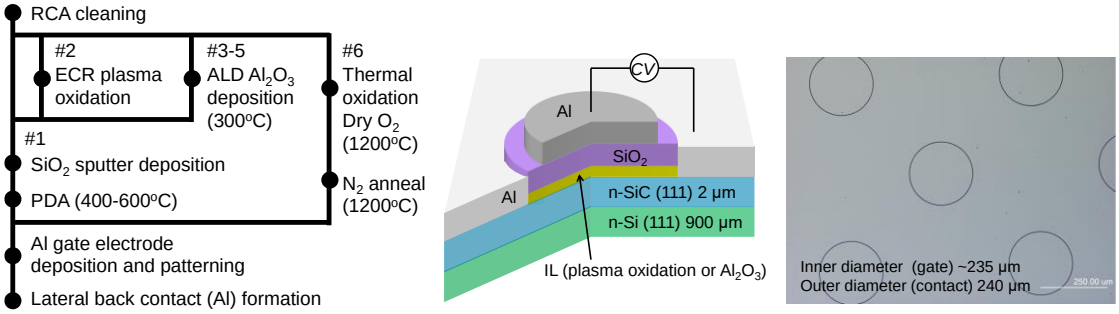


Fig. 1 Sample fabrication procedure, cross-sectional picture of fabricated lateral MOS capacitor, and top-view optical microscope image.

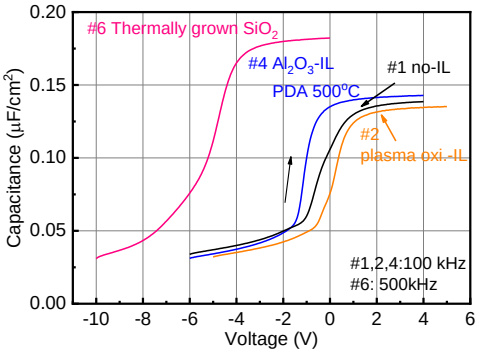


Fig. 2 High frequency *C-V* characteristics for 3C-SiC MOS capacitors with various structures.

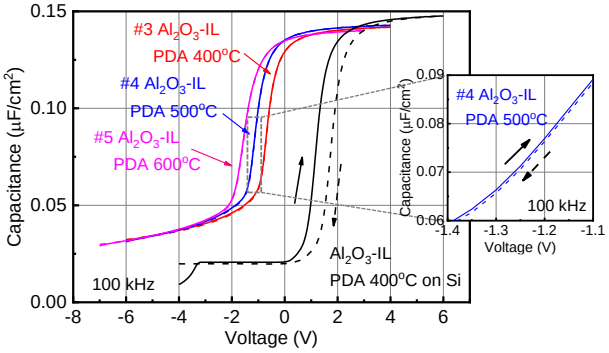


Fig. 3 Bi-directional *C-V* curves of 3C-SiC MOS capacitors with $Al_2O_3$-IL. Hysteresises of 3C-SiC MOSs are negligibly small.

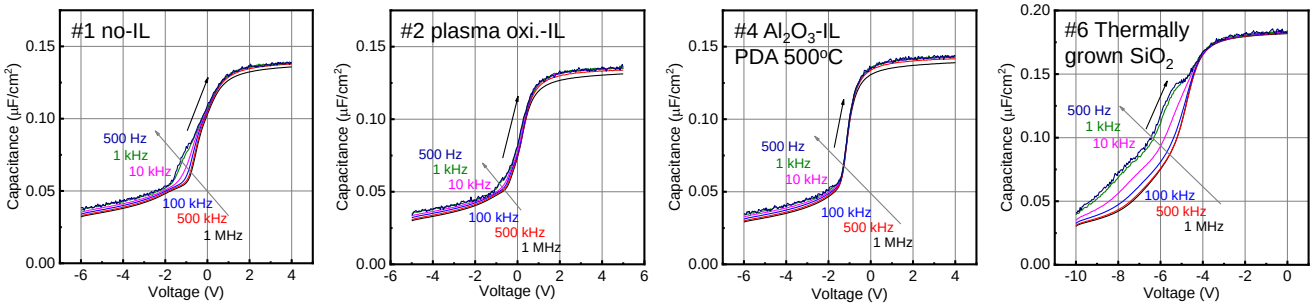


Fig. 4 *C-V* frequency dependence for samples "#1 no-IL", "#2 plasma oxidized-IL", "#4 $Al_2O_3$-IL (PDA 500°C)", and "#6 thermally grown $SiO_2$". Frequency range is 1 M – 500 Hz.

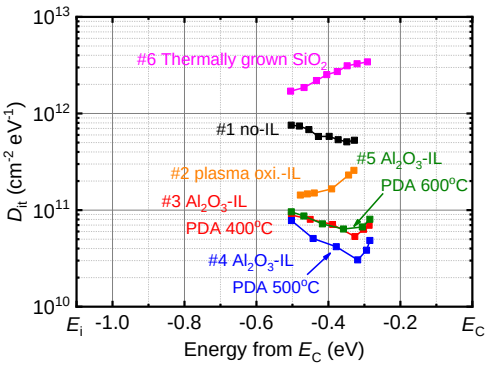


Fig. 5 $D_{it}$ distributions for 3C-SiC MOS capacitors in this study.

## References


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