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Achieving extremely high levels of electrically active doping in silicon carbide epitaxy

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Abstract

The low temperature epitaxy of cubic silicon carbide (3C-SiC) offers a route to the low-cost integration of the wide bandgap semiconductor into the silicon (Si) industry and enables the use of standard Si based dopants. As a consequence, extremely high levels of electrically active phosphorus dopants have been introduced into 3C-SiC during epitaxial growth with 100% electrical activation up to ~2 × 10^{20} cm^{-3}. The process offers extreme control over the 3C-SiC electrical properties without relying on post-growth ion implantation and very high temperature annealing. Low temperature epitaxy enables the growth of doped 3C-SiC on silicon-on-insulator (SOI) substrates for device applications at high temperatures, avoiding the issue of leakage current into the Si substrate.

1. Introduction

Silicon carbide (SiC) is a wide bandgap semiconductor which can operate at high temperatures and resist chemicals and radiation, making it ideal for applications in a range of harsh environments [1]. Cubic silicon carbide (3C-SiC) can be heteroepitaxially grown on Si, however, there are still no commercial 3C-SiC devices available due to its cost and issues with growth and leakage currents [2]. While leakage into the underlying Si can be managed by transferring the 3C-SiC layer to an insulating substrate, this process is difficult to scale and integrate into current technologies [3].

Achieving high levels of electrically active dopants in 3C-SiC epilayers is crucial for the formation of low resistance Ohmic contacts, controlling material conductivity and forming more intricate structures such as field effect transistors or PiN diodes. High energy ion implantation is typically employed for SiC polytypes, however, this can be an issue with heteroepitaxially grown 3C-SiC/Si material as the upper annealing temperature is limited by the melting point of the Si wafer. The maximum achievable impurity levels through ion implantation of n- or p-type dopants within 3C-SiC are around 6 × 10^{20} cm^{-3}, however, electrical activation at this level of implantation can be around 12%, saturating the free donors at ~7 × 10^{19} cm^{-3} [4] and leaving a high number of interstitial impurities, clusters and defects in the crystal.

Recently invented, the low temperature growth of 3C-SiC offers a commercially viable, high volume production method for 3C-SiC growth [5]. The process enables the accurate control of the epilayer electrical properties through in-situ doping with standard Si based dopants and also offers the opportunity to grow 3C-SiC on non-standard for SiC substrates such as silicon-on-insulator (SOI) or patterned with SiO_2 wafers.

2. Experimental Details

Growth of 3C-SiC epilayers was carried out on both standard on-axis, p^--100 mm Si (001) and SOI wafers within an ASM Epsilon 2000 RP-CVD system, see Fig. 1. SOI wafers consisted of a 100 nm thick active Si layer with a ~1 µm thick buried oxide (BOX) layer. The resistivity of the 3C-SiC was manipulated through the introduction of varying levels of n-type dopants, in this case phosphorus (P), in-situ during epitaxial growth within a 50 nm thick epilayer. The concentrations of impurities incorporated in the 3C-SiC epilayers were measured using secondary ion mass spectroscopy (SIMS). Other material properties were investigated using a range of techniques including X-ray diffraction (XRD), atomic force microcopy (AFM), scanning electron microscopy (SEM) and transmission electron microscopy (TEM). The electrical properties of the 3C-SiC epilayers and their suitability for use in high temperature devices was analyzed through the fabrication of Hall bar test device structure through standard photolithography, dry etching and metal deposition techniques. Nickel chromium (NiCr) was sputtered onto the n-type 3C-SiC which formed a suitable Ohmic contact to the films without subsequent thermal annealing.

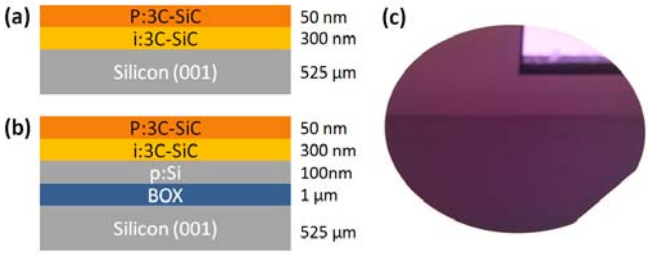

Fig. 1 Cross sectional schematic of 3C-SiC epilayers grown on (a) standard bulk Si (001) and (b) SOI. (c) 3C-SiC/Si (001) epi wafer.

The resistivity and electrically active carrier concentrations of the 3C-SiC were measured within a low temperature cryostat from 300 – 15 K using Hall Effect measurements. Higher temperature electrical measurements were made within a Linkam THMS600 stage from room temperature up to 823 K.

3. Results and Discussions

The introduction of n-type impurities into the 3C-SiC shows an expected impact on the sheet resistance of the Hall bar test devices. Low doped 3C-SiC exhibits high resistance

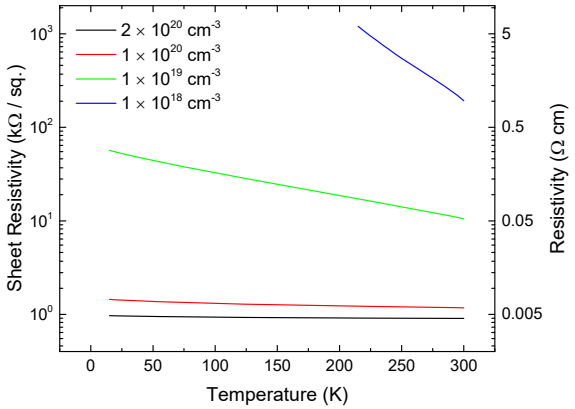

Fig. 2 Sheet resistance and approximate resistivity for 3C-SiC epilayers with different P doping levels.

and strong temperature dependence, while higher doped epilayers show minimal temperature dependence, see Fig. 2. Electrically active dopants up to ~2×10^{20} cm^{-3} were achieved with an ideal linear relationship between impurity and carrier concentration, see Fig. 3. Introducing levels of impurities above 2×10^{20} cm^{-3} led to saturation of carrier concentration and interstitial P within the crystal.

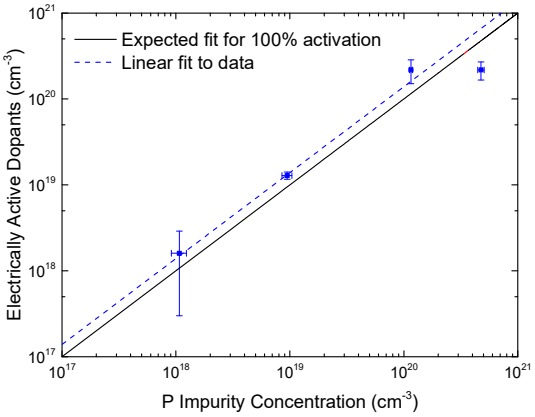

Fig. 3 Comparing electrically active and total incorporation of P in the 3C-SiC epilayers, extracted by Hall Effect measurements and SIMS profiling respectively.

Operating the test devices based on 3C-SiC/Si (001) epi wafers at high temperatures demonstrates the key drawback of these layers for high temperature operation. Current-voltage (I-V) curves lose Ohmic behavior around 200 °C where the path of least resistance through the sample shifts from the 3C-SiC to the junction set up by the 3C-SiC/Si interfaces. Beyond ~250 °C, leakage current through the junction and conductivity of the Si substrate increases to mask all resistive behavior of the 3C-SiC, see Fig. 4. This effect can be mitigated through the use of SOI substrates. By dramatically reducing the thickness of the Si layer in contact with the 3C-SiC, the conductive path through the substrate is reduced. The resistance of a Hall bar fabricated from the doped 3C-SiC/SOI epi wafer shows a linear dependence between resistivity and temperature, see Fig. 4. Cycling this device between 550 °C and room temperature shows no hysteresis or device degradation implying no diffusion of metal or dopants through the 3C-SiC.

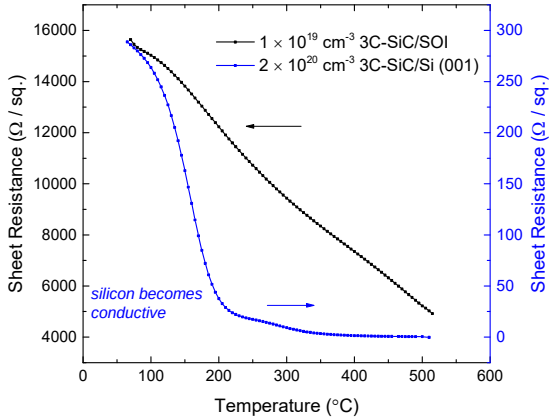

Fig. 4 Temperature dependence of the sheet resistance for the 3C-SiC/Si and 3C-SiC/SOI Hall bars.

4. Conclusions

The electrical properties of 3C-SiC have been manipulated through the introduction of n-type dopants up to ~2×10^{20} cm^{-3} with 100% activation, amongst the highest found in literature, during epitaxy, see Table I. Increasing the P incorporation within the 3C-SiC results in saturation leading to crystal degradation and interstitial P. The increase in electrically active dopants within the 3C-SiC epilayers reduces the temperature sensitivity at both low and high temperatures. At high temperatures, standard 3C-SiC/Si epi wafers present a challenge with current leaking into the substrate. Growing 3C-SiC on SOI can mitigate the leakage effect of the Si. The resistance of devices fabricated from 3C-SiC/SOI remains high at temperatures up to 550 °C and can be manipulated by adjusting the doping levels. Doping is crucial to the use of 3C-SiC within electronic devices in order to form suitable low resistance Ohmic contacts and fabricate device structures such sensors, diodes or MOSFETs.

Table I Typical doping levels achieved in n-type doped 3C-SiC.

Dopant	Method	Impurities (cm^{-3})	Activation (%)	Ref.
N	Ion imp.	6×10^{20}	11.7	[4]
N	Ion imp.	1×10^{20}	60	[6]
N	In-situ	6×10^{18}	100	[7]
P	In-situ	2×10^{20}	100	This work

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