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Low-Temperature Formation of n-Type Ge on Insulator by Thickness-Modulated Sb-Induced Layer Exchange Crystallization Combined with Thin Ge Under-Layer Insertion

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Abstract

Low-temperature (<500°C) formation of n-type crystalline Ge on insulator by Sb-induced crystallization is investigated. It is found that by annealing of a-Ge (100 nm)/Sb (100 nm) stack structures, dominant constituents of top and bottom layers change into Sb and Ge, respectively. However, a large amount of Sb (~20%) remains at the bottom-layer/substrate interface. Moreover, the film thickness significantly decreases by Ge/Sb evaporation triggered by excess Sb during annealing. To solve these problems, we decrease the Sb thickness to 50 nm, and introduce a thin a-Ge under-layer (5 nm) between the bottom-layer/substrate interfaces. This enables low-temperature formation (450ºC) of n-type crystalline Ge without evaporation or residual Sb at bottom-layer/substrate interface.

1. Introduction

Low temperature (<500ºC) formation of n-type crystalline Ge films on insulator is necessary to achieve next-generation large-scale integrated circuits (LSIs) with multi-functions. This is because n-type Ge shows higher-efficiency of optical functions owing to high electron population in the Γ band.

To obtain crystalline Ge on insulator at low temperature, various techniques have been developed [1]. Among them, we have focused on the metal-induced layer-exchange crystallization (MIC), where Al [2,3] or Au [4] is employed as catalyst. This is because orientation-controlled large-grain crystals (>10μm) are obtained by combining with interface layer modulation [2-4]. However, all of the Ge films grown by the previously-reported MIC show p-type conduction due to the residual Al or vacancy-related defects. Thus, a novel technique should be developed to obtain n-type Ge. In the present study, we investigate layer-exchange crystallization of Ge by using a new catalyst, i.e., a group V element Sb, to achieve n-type Ge on insulator at low temperatures.

2. Experiments and Results

The sample structure illustrated in Fig. 1 was investigated firstly. As shown in Fig. 1, stack structures of a-Ge/Sb (thickness: 100/100 nm) were formed on quartz (SiO_2) substrates. The samples were annealed at 300ºC−450ºC in N_2 to induce crystallization. The Raman spectra before and after annealing are shown in Fig. 2, where the measurements were performed from top and back sides of the samples. It clearly indicates that after annealing (450ºC, 20 h), a strong peak due to Sb-Sb bonding (~150 cm^{-1}) is observed from the top side, and a large peak due to Ge-Ge bonding (~300 cm^{-1}) is observed from the back side. This suggests layer-exchange crystallization of Ge by annealing (450ºC, 20 h).

The composition profiles measured by Auger electron spectroscopy (AES) of samples before and after annealing (450ºC, 20 h) are shown in Figs. 3(a) and 3(b), respectively. As shown in Fig. 3(a), a stack structure of Ge/Sb is formed on the substrate before annealing. On the other hand, as shown in Fig. 3(b), after annealing (450ºC, 20 h), Sb and Ge become dominant constituents in the top and bottom layers, respectively. However, the total thickness of the sample has decreased to ~60 nm, which is about one third of the initial thickness, due to thermal evaporation. Moreover, Sb atoms with high concentration (~20%) remain at the bottom-layer/substrate interface.

Since Ge evaporation is not found in SPC of pure Ge at 450ºC [5], the Ge evaporation is attributed to excess Sb atoms. Thus, decrease of Sb thickness is expected to suppress the Ge evaporation. On the other hand, it is reported that introduction of thin Ge under-layer into the initial catalyst/substrate interface enhances the layer-exchange crystallization in AIC [3]. The introduction of thin a-Ge under-layer will be also useful to enhance the layer-exchange in Sb-induced crystallization, which will result in decrease of the remaining Sb atoms at the bottom-layer/substrate interface. Thus, we examine the sample structure shown in Fig. 4, where the thickness of Sb is decreased to 50 nm and a thin a-Ge layer (~5 nm) is inserted between the Sb layer and the substrate.

Raman spectra before and after annealing at 450ºC for 20 h are shown in Fig. 5. After annealing, a strong peak due to Sb-Sb bonding appears on the top side, while a large peak due to Ge-Ge bonding appears on the back side. This suggests the layer-exchange crystallization. The composition profiles before and after annealing (450ºC, 20 h) are shown in Figs. 6(a) and 6(b), respectively. This clearly indicates that layer-exchange crystallization has completed by annealing (450ºC, 20 h). Here, the total thickness (~150 nm) of the sample is the same as that before annealing. Moreover, there are almost no residual Sb at the bottom-layer/substrate interface after annealing.

To investigate electrical properties of the grown layers, selective etching of Sb was performed. AES analysis revealed that the concentration of residual Sb in the grown Ge layer was under detection limit (~1%) after the selective etching of Sb, though Fig. 6(b) indicated high concentration Sb around the interface between the top and bottom layers. This indicates that the high concentration Sb atoms exist at Ge-grain-boundaries in the bottom layer, and can be completely removed by selective etching. The thermo-electro-motive force measurements revealed n-type conduction of the grown Ge layer. Detailed characterization of the electrical and optical properties of the grown layers is underway.

3. Conclusion

Sb-induced crystallization of Ge has been investigated. Annealing (450°C, 20 h) of a-Ge (100 nm)/Sb (100 nm) stacked structures resulted in Ge evaporation and residual Sb atoms at the bottom-layer/substrate interface. To solve the problems, decrease of Sb thickness to 50 nm and introduction of thin Ge under-layer (5 nm) were examined. This enabled layer-exchange growth without Ge evaporation or residual Sb at the bottom-layer/substrate interface. As a result, n-type Ge on insulator has been obtained at a low temperature (450°C). This technique will facilitate realization of advanced LSIs merged with optical functions.

References

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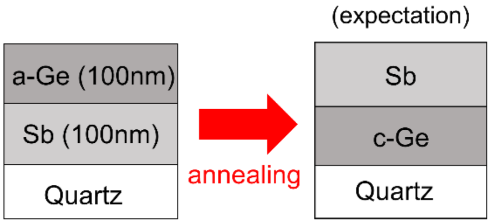

Fig.1. Schematic sample structure.

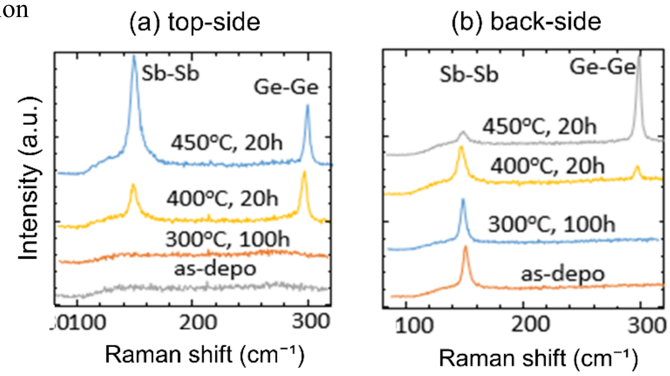

Fig.2. Raman spectra obtained from top-side (a) and back-side (b) of samples before and after annealing. Initial a-Ge/Sb film thicknesses are 100/100 nm.

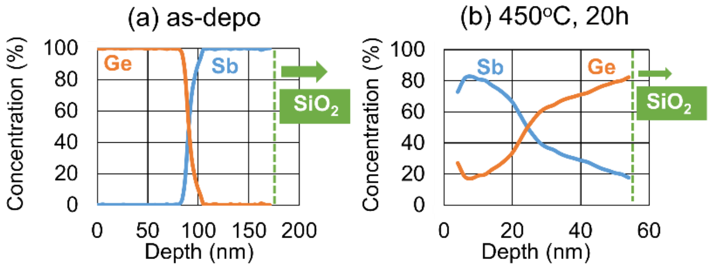

Fig.3. In-depth profiles of Ge and Sb concentrations in samples before (a) and after annealing (450°C, 20h) (b). Initial a-Ge/Sb film thicknesses are 100/100 nm.

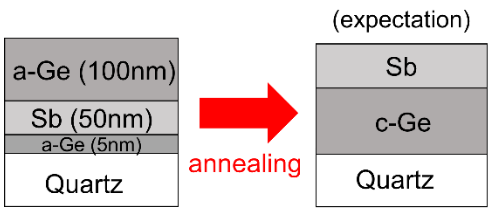

Fig.4. Schematic of modified sample structure.

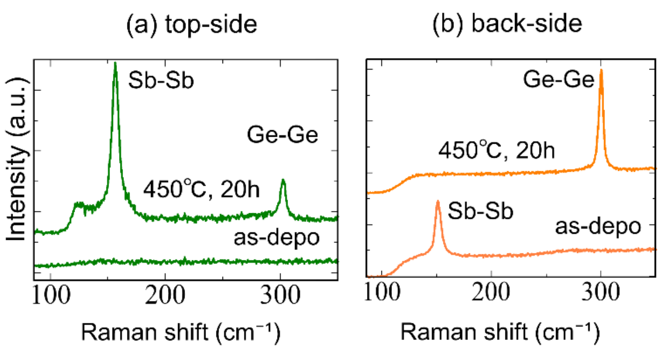

Fig.5. Raman spectra obtained from top-side (a) and back-side (b) of samples (a-Ge/Sb/a-Ge=100/50/5 nm) before and after annealing (450°C, 20 h).

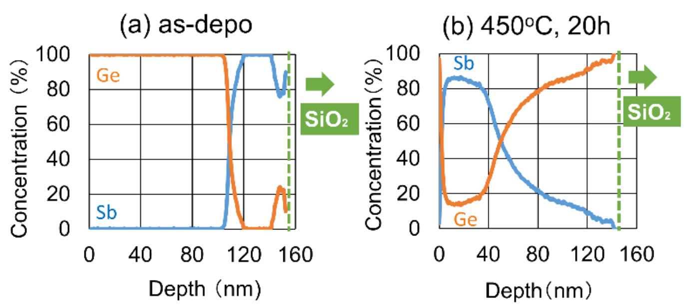

Fig.6. Composition profiles of samples (a-Ge/Sb/a-Ge=100/50/5 nm) before (a) and after annealing (450°C, 20h) (b).