High-quality diamond epitaxial layer growth and electron devices application

Y. Koide, J. Liu, M. Imura, and M.Y. Liao

National Institute for Materials Science (NIMS) 1-2-1, Sengen, Tsukuba Ibaraki 305-0044, Japan Phone: +81-29-8512270 E-mail: koide.yasuo@nims.go.jp

Abstract

Diamond is a candidate material for next-generation power electronics and integrated circuit which operate under extreme environment. In order to use an advantage of high-density hole channel of hydrogenated diamond surface, we have developed the high-k stack gate dielectrics for H-diamond MOSFETs, such as HfO₂/HfO₂, LaAlO₃/Al₂O₃ Ta₂O₅/Al₂O₃, and ZrO₂/Al₂O₃, TiO₂/Al₂O₃, and AlN/Al₂O₃ prepared by a combination of sputter-deposition (SD) and atomic layer deposition (ALD) techniques.

1. Introduction

Semiconductor diamond has long been studied for applications in high-power and high-frequency electronic devices because it offers wide bandgap energy, high breakdown field, high carrier mobility, and high thermal conductivity. However, diamond electronic device development has been limited by the low free carrier density that occurs in diamond at room temperature because of high activation energies of dopants. Fortunately, hydrogenated diamond (H-diamond) can accumulate two-dimensional hole gases on its surface with a sheet hole density of 10¹²-10¹³ cm⁻². Notably, after the H-diamond is exposed to a NO₂ ambient or annealed in a NH₃+H₂ ambient, the hole density increased to a value as high as 10^{14} cm^{-2} [4,5]. The H-diamond is therefore considered to be a promising channel layer for high performance diamond electronic device fabrication. Recently, high-performance H-diamond-based metal-semiconductor field-effect transistors metal-oxide-semiconductor (MESFETs) and FETS (MOSFETs) have been fabricated. Because insulating passivation layers are present between the gate metals and the Hdiamond channel layers, the leakage current densities of the resulting MOSFETs are lower than those of the MESFETs.

Several insulating materials, including SiO₂ [1], CaF₂ [2], and Al₂O₃ [3] have been deposited on the H-diamond layer for MOSFETs. The current output of Al₂O₃ on the NO₂treated H-diamond channel layer was reported to be as high as 1.35A/mm [4]. Recently, to response a high H-diamond channel hole density (10^{14} cm⁻²) under a small applied electrical field, we have developed high-k insulators on H-diamond for both MOS capacitors and MOSFETs [6–11]. In this talk, we will review our work for developing oxide and nitride gated H-diamond MOSFETs using high-quality diamond epilayer grown by a microwave-plasma chemical deposition technique.

2. Results and Summary

The high-k insulators, which have a bilayer structure, were deposited by radio-frequency (RF) sputter deposition (SD) and atomic layer deposition (ALD) techniques. The thin ALD-insulator layer was deposited as a buffer layer to protect the hydrogen surface from an SD plasma discharge damage during SD insulator deposition on the H-diamond surface. SD-HfO₂/ALD-HfO₂ [6], SD-LaAlO₃/ALD-Al₂O₃ [7] SD-Ta₂O₅/ALDAl₂O₃ [8], SD-ZrO₂/ALD-Al₂O₃ [9], and SD-TiO₂/ ALD-Al₂O₃ [10] layers have been deposited on H-diamond for the MOSFETs. All of these MOSFETs showed good operating performance with distinct pinch-off characteristics.

Figure 1(a) shows J as a function of the electric field for H-diamond MOS capacitors with the different oxide insulators as dielectric layers. The electric field is determined by dividing the gate voltage by the insulator thickness [6–11]. It was observed that the J values of MOS capacitors at 1.5 MV/cm and 1.5 MV/cm are different. The asymmetry of J is possibly attributed to work function difference between gate metal and H-diamond channel layer, accumulation of holes at the oxide/H-diamond interface, and trapped charges in the metal/oxide/H-diamond structures. The J values for the MOS capacitors at an electric field of 1.5 MV/cm are summarized in Table I. The SD-TiO₂/ALD-Al₂O₃/H-diamond and SD-LaAlO₃/ALD-Al₂O₃/H-diamond MOS capacitors show the highest and lowest leakage current densities of 7.3x10⁻³A cm⁻ ² and 6.9x10⁻⁹A cm⁻², respectively. The J value of the ALD-TiO₂/ALD-Al₂O₃/H-diamond MOS capacitor is approximately 2.1×10^{-5} A cm⁻², which is lower than the corresponding values for the SD-ZrO₂/ALD-Al₂O₃/H-diamond [9], SD-Ta₂O₅/ALD-Al₂O₃/H-diamond [8], and SDTiO₂/ALD-Al₂O₃ /H-diamond MOS capacitors. Although the SD-LaAlO₃ /ALD-Al₂O₃/H-diamond [7], ALD-Al₂O₃/H-diamond [11], and SD-HfO₂/ALD-HfO₂/H-diamond [6] MOS capacitors show lower leakage current densities than that of the ALD-TiO₂/ALD-Al₂O₃/H-diamond MOS capacitor, the C_{max} and k values of these capacitors are all lower than 0.26 μ F/cm² and 9.4, respectively. Among the various MOS capacitors, the ALD-TiO₂/ALD-Al₂O₃/H-diamond device has the highest values of C_{max} and k.

Figure 1(b) summarized the log $|I_{DS}|$ -V_{GS} characteristics of the MOSFETs with different oxide insulators [6–11]. Since there are no interspacing between source/drain and gate, the on-resistances for the SD-ZrO₂/ALD-Al₂O₃/H-diamond [9] and SD-Ta₂O₅/ALD-Al₂O₃/H-diamond [8] MOSFETs are much lower than other insulator/H-diamond MOSFETs, which leads to their higher $I_{DS,max}$. However, the on/off ratios for them are much lower than other MOSFETs. In our previous studies, we first demonstrated the fabrication of H-diamond MOSFETs with enhancement mode characteristics [6, 7]. There are two necessary conditions required to achieve enhancement mode characteristics for these H-diamond MOSFETs, which are annealing of the MOSFETs in the 180-300 C range and use of SD-insulator/ALD-insulator bilayer structures [11]. Therefore, the SD-LaAlO₃/ALD-Al₂O₃/H-diamond [7]. SD-HfO₂/ALDHfO₂/ H-diamond [6], and SD-TiO₂/ALD-Al₂O₃/H-diamond MOSFETs operate with enhancement mode characteristics. Otherwise, due to the lack of annealing process or bilayer oxide insulator structure, the SD-Ta₂O₅/ALD-Al₂O₃/H-diamond [8], SD-ZrO₂/ALD-Al₂O₃ /H-diamond [9], and ALD-Al₂O₃/H-diamond MOSFETs operate with depletion mode characteristics. In this study, we have fabricated an ALD-TiO2/ALD-Al2O3/H-diamond MOS-FET with enhancement mode characteristics. Therefore, the conditions for enhancement mode H-diamond MOSFET fabrication can be updated. After annealing, both the SD-insulator/ALD-insulator and ALD insulator/ALD-insulator bilayer structures on the H-diamond channel layers can make the MOSFETs operate with enhancement mode characteristics. Among different insulator/H-diamond MOSFETs, the SS for the ALD-TiO₂/ALD-Al₂O₃/H-diamond MOSFET is the lowest. The ALD-Al₂O₃/H-diamond and ALD-TiO₂/ALD-Al₂O₃ /H-diamond MOSFETs show lower Dit than other SD-insulator/ALD-insulator/H-diamond MOSFETs. Therefore, during the deposition of SD-insulators by sputtering process, there is possibly some plasma damage or SD-insulator diffusion effect for the ALD-insulator/H-diamond interfaces, which leads to the higher D_{it}.

References

[1] T. Saito, K. H. Park, K. Hirama, H. Umezawa, M. Satoh, H. Kawarada, Z.Q. Liu, K. Mitsuishi, K. Furuya, and H. Okushi, J. Electron. Mater. 40, 247 (2011).

[2] Y. Otsuka, S. Suzuki, S. Shikama, T. Maki, and T. Kobayashi, Jpn. J. Appl. Phys., Part 1 34, L551 (1995).

[3] K. Hirama, H. Sato, Y. Harada, H. Yamamoto, and M. Kasu, Jpn. J. Appl. Phys. 51, 090112 (2012).

[4] H. Sato and M. Kasu, Diamond Relat. Mater. 31, 47 (2013).

[5] M. Imura, R. Hayakawa, H. Ohsato, E. Watanabe, D. Tsuya, T. Nagata, M. Y. Liao, Y. Koide, J. Yamamoto, K. Ban, M. Iwaya, and H. Amano, Diamond Relat. Mater. 24, 206 (2012).

[6] J. W. Liu, M. Y. Liao, M. Imura, and Y. Koide, Appl. Phys. Lett. 103, 092905 (2013).

[7] J. W. Liu, M. Y. Liao, M. Imura, H. Oosato, E. Watanabe, A. Tanaka, H. Iwai, and Y. Koide, J. Appl. Phys. 114, 084108 (2013).

[8] J. W. Liu, M. Y. Liao, M. Imura, E. Watanabe, H. Oosato, and Y. Koide, J. Phys. D.: Appl. Phys. 47, 245102 (2014).

[9] J. W. Liu, M. Y. Liao, M. Imura, A. Tanaka, H. Iwai, and Y. Koide, Sci. Rep. 4, 6395 (2014).

[10] J. W. Liu, M. Y. Liao, M. Imura, R. G. Banal, and Y. Koide, J. Appl. Phys. 121, 224502 (2017).

[11] J. W. Liu, M. Y. Liao, M. Imura, T. Matsumoto, N. Shibata, Y. Ikuhara, and Y. Koide, J. Appl. Phys. 118, 115704 (2015).



Fig. 1. (a) Summary of leakage current densities for the different oxide insulators on H-diamond for the MOS capacitors. (b) Summary of log $|I_{DS}|$ -V_{GS} characteristics of the MOSFETs with different oxide insulators.

Table I. Summary of electrical properties for the H-diamond MOS capacitors and MOSFETs with the different oxide insulators as dielectric layers. The J values for the MOS capacitors are the ones at an electric field of 1.5 MV/cm.

Material Buffer layer	SD-LaAlO ₃ ALD-Al ₂ O ₃	ALD-Al ₂ O ₃	SD-HfO ₂ ALD-HfO ₂	ALD-TiO ₂ ALD-Al ₂ O ₃	SD-ZrO ₂ ALD-Al ₂ O ₃	SD-Ta ₂ O ₅ ALD-Al ₂ O ₃	SD-TiO ₂ ALD-Al ₂ O ₃
$J (\mathrm{A \ cm^{-2}})$	6.9×10^{-9}	$1.1 imes 10^{-7}$	$8.4 imes 10^{-7}$	$2.1 imes 10^{-5}$	$1.0 imes 10^{-4}$	$7.6 imes 10^{-4}$	$7.3 imes 10^{-3}$
$C_{\rm max}$ ($\mu \rm F cm^{-2}$)	0.26	0.19	0.24	0.83	0.31	0.40	0.73
k	9.1	5.4	9.4	27.2	12.8	12.7	22.5
$I_{\rm DS,max}$ (mA mm ⁻¹)	-7.5	-22.8	-24.9	-11.6	-224.1	-94.3	-12.1
On/off	2.1×10^{9}	$>9.1 \times 10^{5}$	$6.6 imes 10^8$	$8.3 imes 10^8$	$4.0 imes 10^4$	$1.7 imes 10^4$	$1.0 imes 10^9$
$V_{\rm TH}$ (V)	-3.6 ± 0.1	3.8 ± 0.1	-1.3 ± 0.1	-0.8 ± 0.1	1.4 ± 0.1	1.3 ± 0.1	-0.9 ± 0.1
$SS (mV dec^{-1})$ $D_{it} (eV^{-1} cm^{-2})$	$220 \\ 2.38 \times 10^{12}$	$138 \\ 1.58 \times 10^{12}$	$195 \\ 3.44 \times 10^{12}$	$79 \\ 1.74 \times 10^{12}$	$206 \\ 4.81 \times 10^{12}$	$244 \\ 7.81 \times 10^{12}$	$115 \\ 4.30 \times 10^{12}$