Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp411-412

Similarity of Potential-Induced Degradation in Superstrate-Type Thin-Film Si and CdTe Photovoltaic Modules

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Abstract

Degradation phenomena under high-voltage stress, called potential-induced degradation (PID) in general, were studied in superstrate-type photovoltaic (PV) modules, such as thin-film Si and CdTe modules. Both deterioration in PV performances and delamination of transparent conducting oxide (TCO) layer on glass substrate were in common observed for both PV modules. Humidity remarkably accelerated the delamination. These findings suggest that the common origin of PID for superstrate-type PV modules is damage and delamination of TCO layer.

1. Introduction

Potential-induced degradation (PID) has attracted much attention due to a dramatic decrease in output power within relatively short period. However, degradation behavior strongly depends on kinds of photovoltaic (PV) cells. There are many reports on PID for crystalline Si solar cells and various characteristic features of PID for conventional p-type, front-emitter n-type, rear-emitter n-type, heterojunction n-type, and interdigitated back-contact n-type crystalline Si PV modules have been reported. On the other hand, there are only a few reports on thin-film PV modules, especially, superstrate-type PV modules, such as thin-film Si [1] and CdTe [2] modules. There are large differences in module structures between these superstrate-type type PV modules and crystalline Si or $Cu(In,Ga)Se_2$ PV modules. Namely, the encapsulant exists between the cover glass and the PV cell in the latter case, on the other hand, the cover glass, which is the source of Na, possible origin of PID, directly contacts to the PV cell in the former case. Therefore PID behavior may be much different between them. It is also pointed out that improved encapsulant cannot prevent PID in the former case although employment of newly developed encapsulant with high tolerance to PID is one of the popular methods for preventing PID in the latter case. In this study, typical superstrate-type thin-film PV modules, tandem-type of hydrogenated amorphous Si and hydrogenated microcrystalline Si (a-Si:H/μc-Si:H) and CdTe PV modules, were subjected to PID test with high-voltage stress and their PID behaviors were compared.

2. Experimental

Superstrate-type a-Si:H/μc-Si:H and CdTe PV modules were fabricated by vacuum lamination using the PV cell formed on cover glass, fast-cure type ethylene-vinyl acetate (EVA) encapsulant, and polyvinyl fluoride (PVF)/polyethylene terephthalate (PET)/PVF triple-layer back sheet. Both the encapsulant and the back sheet were used for the back side. These PV modules were subjected to indoor PID acceleration test using Al plate. PID tests were carried out in the dry chamber at 85℃ and very low relative humidity below 2%. Both p and n electrodes of PV cells were shorted and negative or positive high voltage, typically ±1000 or 2000 V, was applied between shorted electrodes and grounded Al plate. Before and after PID tests current-voltage (*I*-*V*) characteristics of the PV modules were measured using pulsed solar simulator at 25℃.

3. Results and discussion

Figure 1 shows the short-circuit current (I_{sc}), open-circuit voltage (V_{oc}), fill factor (FF) and maximum power (P_{max}) for a-Si:H/μc-Si:H and CdTe PV modules as a function of PID test time. In this case negative voltage of -2000 V was applied. I_{sc} shows relatively large decrease in CdTe modules, on the other hand, both V_{oc} and FF show larger decrease for a-Si:H/μc-Si:H modules than CdTe modules. However, extent of decrease in P_{max} with test time is roughly similar in both modules. Recovery from PID was also observed by positive high-voltage application for both modules. However, much more drastic PID was observed after the second PID test following almost the complete recovery, as shown in Fig. 2. For a-Si:H/μc-Si:H modules, positive high voltage of +1000 V was applied before PID test. In this case drastic reduction in P_{max} is observed in comparison with PID test of -1000 V without positive voltage application before PID test, as shown in Fig. 2 (a). These facts mean that recovery from PID is accomplished by positive voltage application; however, such recovery leads to low tolerance to PID. Figure 3 (a) shows photographs of the delamination by indoor PID test for a-Si:H/μc-Si:H modules. Similar delamination was also observed for CdTe modules. It was confirmed that such delamination occurs in SnO_2:F transparent conducting oxide (TCO) layer. In outdoor exposure shown in Fig. 3(b), such line-shape delamination often starts from the location near the bottom frame, where rainwater is easy to remain. Also in indoor PID tests, delamination widely expanded and rapidly progressed for both a-Si:H/μc-Si:H and CdTe modules by leaving those in the

environment with usual humidity after taking out those from the dry chamber for PID test with relative humidity below 2%. It is suggested from these findings that the delamination is much promoted by water vapor infiltrating into the modules. It is possible that the delamination of TCO is common origin of PID for superstrate-type thin-film PV modules although degradation behavior in the initial stage of PID test reflects the nature or the difference of each cell type, such as thin-film Si and CdTe.

4. Conclusions

It was found that PID behavior for superstrate-type thin-film PV modules, such as thin-film Si and CdTe modules, are mainly governed by delamination of TCO layer. Improvement of TCO layer, especially high tolerance to infiltrated water vapor, is key factors for realizing highly reliable thin-film Si and CdTe PV modules against PID.

Acknowledgements

This work was supported by the New Energy and Industrial Technology Development Organization.

References

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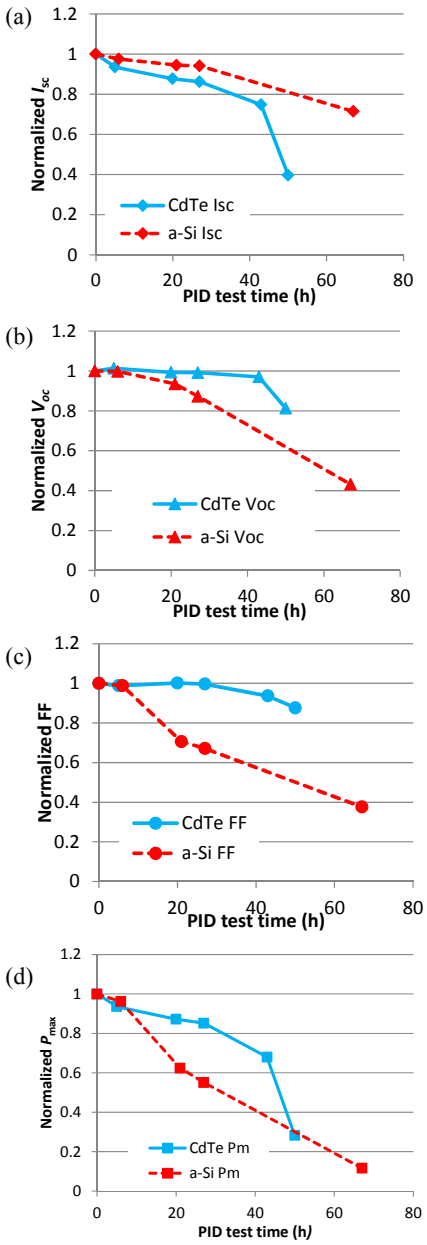

Fig. 1 Normalized I_{sc} (a), V_{oc} (b), FF (c) and P_{max} (d) for a-Si:H/μc-Si:H and CdTe PV modules as a function of PID test time.

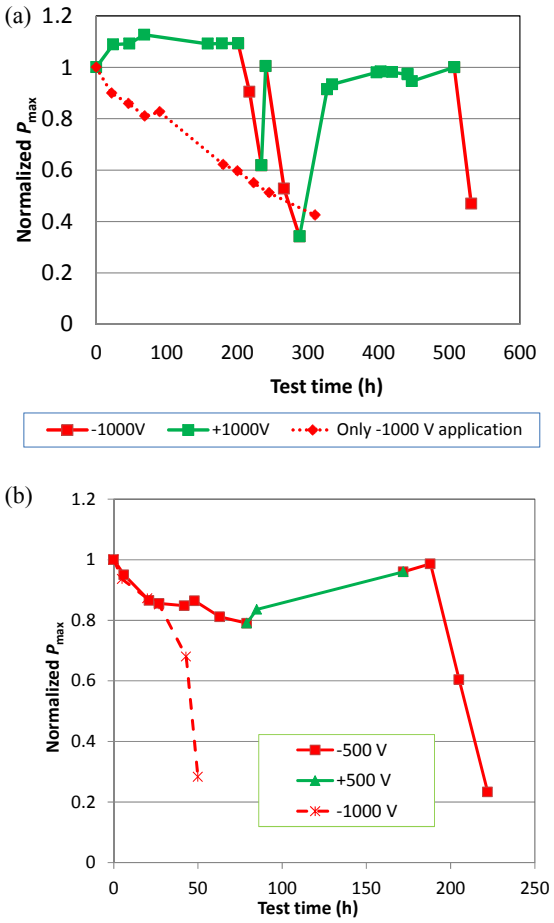

Fig. 2 Normalized P_{max} for a-Si:H/μc-Si:H (a) and CdTe (b) PV modules as a function of test time. Green and red symbols and guides for eye represent positive and negative voltage applications, respectively.

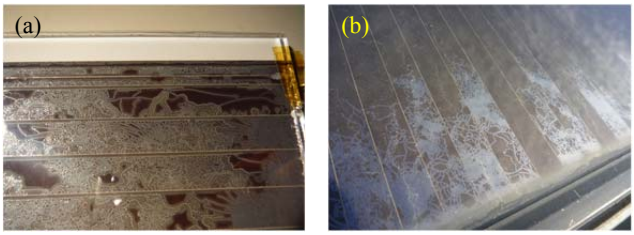

Fig. 3 Appearance of delamination observed for a-Si:H/μc-Si:H PV modules after indoor PID test (a) and outdoor exposure (b).