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Optimum substrate design of planar type Si nanowire thermoelectric generator

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Abstract

We computationally demonstrate that reducing the parasitic thermal resistance of substrate is an effective way for improving the power density of planar silicon nanowire thermoelectric generators (SiNW TEGs). The heat flow in the substrate is controlled by replacing a part of Si substrate with SiO_2 or Cu with a different thermal conductivity. It was found that, not only beneath the cold side edge of SiNW, replacing the whole substrate by Cu is the most effective way to improve the power generation density. The results show that the parasitic thermal resistance of the entire substrate should be suppressed as a matter of first priority.

1. Introduction

Energy harvester, which generate an electric power from ambient energy sources, is a key device for realizing the trillion sensor network society. Thermoelectric generator (TEG) is an ultimate energy harvester which can utilize ubiquitous heat energies. Recently, Si nanowires (SiNWs) emerged as a promising thermoelectric material [1], thanks to their low thermal conductivity [2, 3]. Si based micro TEG is advantageous because it can be fabricated by the conventional CMOS process [4, 5].

In this study, we pursued an optimum substrate structure by means of TCAD simulation in order to create a large temperature difference across SiNWs.

2. Experimental method

Fig.1 (a) and 1(b) shows the unit structure of the planar SiNW TEG and the cross-sectional view. The thicknesses of Al, AlN, NiSi, SiNWs, SiO_2 layers are set to 100 nm, 550 nm, 50 nm, 50 nm, 145 nm, and 50 μm, respectively. The width and pitch of SiNWs are 100 nm and 400 nm, respectively. The length of SiNWs and the NiSi pad between them is fixed to 200 nm. As shown in Fig.1 (b), the substrate is divided into three regions (sub 1, sub 2, and sub 3). By changing the material of each region, we prepared various samples structures. The substrate structure is described as the materials of sub1-sub 2-sub 3. In this work, we prepared Si-Si-Si, Si-Si-Cu, Cu-Si-Si, Ox-Si-Cu, Cu-Si-Ox, Cu-Si-Cu and Cu-Cu-Cu substrates, where SiO_2 is expressed as Ox. The thermal conductivities of Cu, Si, SiO_2 and SiNWs are set to 400 W/mK, 131 W/mK, 1.4 W/mK and1.4 W/mK, respectively. Heat transport calculation based on the Fourier rule was conducted by using the finite element method of COMSOL simulator.

3. Results and Discussion

Fig. 2 shows the temperature profiles in the SiNW on substrates of Si-Si-Si, Si-Si-Cu and Cu-Si-Si. The temperature difference is increased by replacing Si region with Cu. The result of the case Si-Si-Cu was almost the same as that of Cu-Si-Si.

Fig.3 summarizes the temperature differences across the SiNW for all samples. Fig.4 shows temperature maps around the n-type SiNW on Ox-Si-Cu, Cu-Si-Ox, and Cu-Si-Cu. No significant difference is observed between Ox-Si-Cu and Cu-Si-Ox. The temperature difference in Cu-Si-Cu is larger than those in Ox-Si-Cu and Cu-Si-Ox, indicating that the larger the temperature difference is established by replacing the more Si regions by Cu.

Fig.5 visualizes the heat flow in the devices on Ox-Si-Cu and Cu-Si-Ox. In the case of Ox-Si-Cu, the heat flux concentrates at sub 3, whereas it is concentrated at sub 1 in the case of Cu-Si-Ox. In spite of the difference in the heat flux distribution in substrate, unexpectedly, the heat flux profile in SiNW does not change as shown in Fig. 6. This is caused by the presence of SiO_2 layer underneath the SiNWs. The SiO_2 layer has high thermal resistance and it almost determines the temperature difference across SiNW.

To increase the temperature difference, it is effective to cool the backside interface of the SiO_2 layer. Fig.7 shows the relationship between the temperature difference across

SiNWs and the thermal resistance of substrate. The temperature difference is almost determined by the thermal resistance of the substrate. It increases as the thermal resistance of the substrate is reduced.

The results indicate that reducing the parasitic thermal resistance of the substrate is more effective than controlling the heat flow of the substrate. Therefore, in order to increase the temperature difference across SiNWs, it is important to cool the SiO_2 layer by lowering the parasitic thermal resistance of the substrate.

4. Conclusions

The simulation results show that the heat flux flowing through the SiNWs does not change greatly even if the heat flow is controlled by providing a high thermal conductivity region or a low thermal conductivity region on the substrate, which is owing to the large thermal resistance of the SiO_2 layer. In order to improve the power generation performance of the planar SiNW TEG, it is important to reduce the parasitic thermal resistance of the substrate for cooling the SiO_2 layer.

Acknowledgements

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Reference

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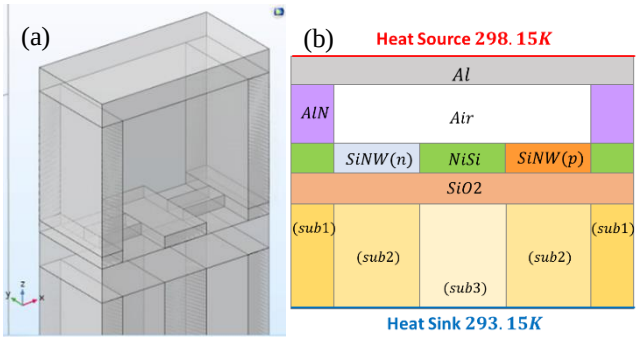


Fig.1 (a) Schematic illustration of the SiNW TEG model (b) Cross-sectional view of device

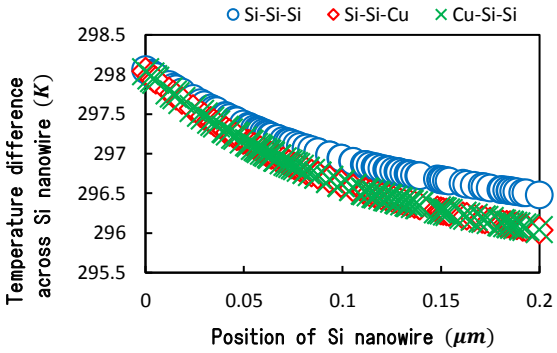


Fig.2 Comparison of temperature profile across SiNW in Si-Si-Si, Si-Si-Cu and Cu-Si-Si.

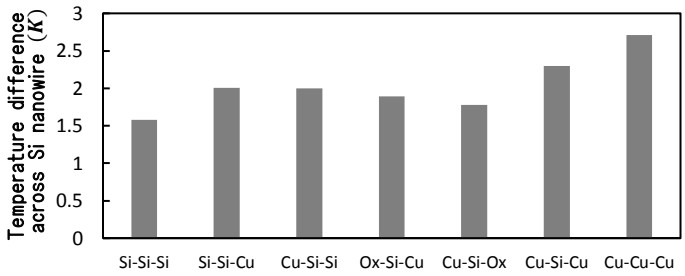
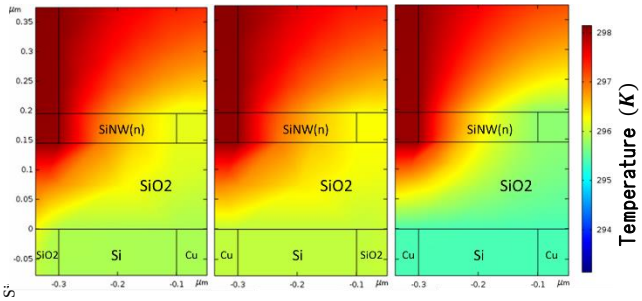
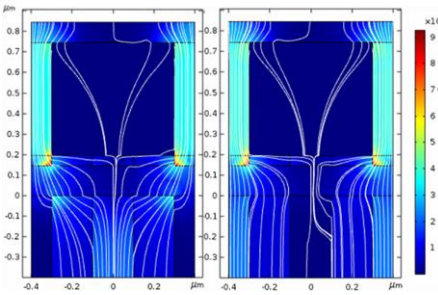


Fig.3 Comparison of temperature difference across SiNW on each substrate



(Ox-Si-Cu) (Cu-Si-Ox) (Cu-Si-Cu)

Fig.4 Temperature map around n-type SiNW.



(Ox-Si-Cu) (Cu-Si-Ox)

Fig.5 The magnitude and flow of heat flux

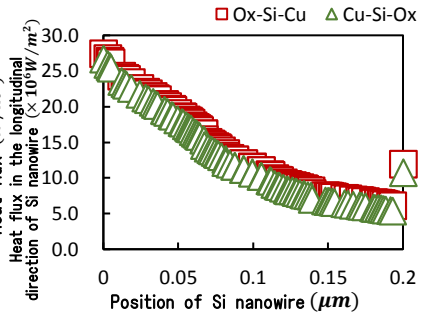


Fig.6 The magnitude of heat flux across SiNW

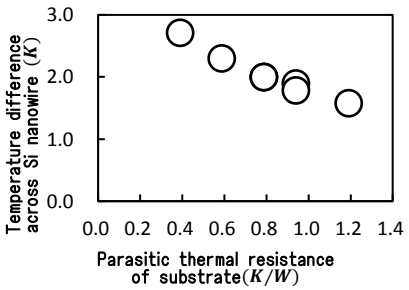


Fig.7 Relationship between parasitic thermal resistance of substrate and temperature difference across SiNW