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Enhancement of Uni-leg Si Thermoelectric Generator Performance by Phononic Crystal Nanostructures

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Abstract

We demonstrate the uni-leg thermoelectric generator fabricated on a silicon membrane. In the device, we introduced phononic crystals known for the effective nanostructures to improve material figure of merit. We measured 7 times larger output power in the device with phononic crystals.

1. Introduction

In the upcoming society of Internet of Things (IoT) many of devices must be powered by themselves, so that autonomous power generators attract large interests. Thermoelectric generators (TEGs) are one of the promising device for IoT society. Many studies have reported the improvement of thermoelectric figure of merit, $ZT = \sigma S^2 T/\kappa$ defined with electrical conductivity σ, Seebeck coefficient S, thermal conductivity κ, and temperature T. In past few decades, many works focused on the nanostructured thermoelectric materials, and achieved strongly reduced κ by nanostructures and improved *ZT* [1].

In this paper, we demonstrate the strong enhancement of TEG performance fabricated in the silicon membrane with phononic crystal (PnC) nanostructures. Since silicon is regarded as a good material for energy harvesting, thus many kinds of silicon nanostructure such as nanowires [2], porous membranes [3], and silicon PnCs [4,5] are studied. Particularly, the PnCs can effectively improve ZT, because in PnCs phonons are well scattered while keeping electron conductive. Although many studies claimed a ZT improvement by PnCs, performance of TEG with PnC was not revealed yet. Here, we experimentally studied impact of PnC nanostructuring on TEG performance and showed the large enhancement of the output power.

2. Method of approach

Sample fabrication

We fabricated Uni-leg (mono-doped) TEGs in SOI wafers composed of 300 nm thick n-type polycrystalline Si active layer and 2.5 μm BOX layer on Si substrate. The uni-leg TEG is fabricated with one ion implantation, two lithography, one metal deposition, and 2 etchings, in total 6 steps which is much less than the steps for typical membrane based TEG fabrication [6]. First, we doped top poly-Si layer of SOI wafer with phosphorous ion implantation and thermal annealing. Next, we created PnC nanostructures by RIE/ICP Si etching with EB lithography mask and Au deposition for wire and electrode was followed. Finally, we removed BOX layer by using vapor phase HF etching except both ends of each unit to keep suspension. In the same process, samples without PnCs were also fabricated as the references.

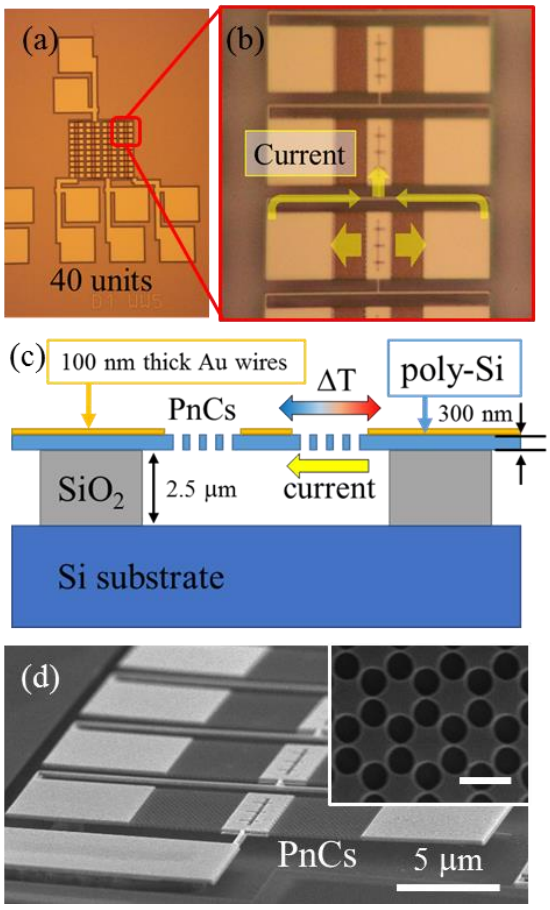

Fig. 1 Microscope images of (a) 40 units with electrodes and (b) 3 units of TEG. (c) Schematic picture for cross-section of one unit. Top poly-Si layer is suspended to create in-plane direction of temperature difference. (d) An SEM image of tilted TEG units shows suspended structure and inset shows PnC nanostructures with 500 nm length scale bar.

Measurement

We measured total resistance of 10, 20, and 40 units in series connection with typical four probes setup. In order to measure the output power of TEGs, we put sample on the heating stage and heated substrate. While both ends of unit are heated through SiO_2 connected with substrate, suspended center of unit is cooled by air convection. As a result, some temperature difference is created in PnCs region, and we can measure output power of TEGs. We changed ΔT between Si substrate and air from -10 to 40 K and measured thermoelectric voltages.

3. Results

The total resistance is proportional to the number of units, and the resistance of one unit is calculated as ~185 Ω and ~97 Ω for PnC samples and membrane samples respectively. Figure 2(a) shows the open circuit voltage as function of set temperature difference ΔT_{SET} between substrate and ambient air. The voltage induced in PnC device shows four times larger than membrane device because of high thermal resistance of PnC structure creating large temperature difference. We calculated the output power per unit area from measured resistance of unit device and voltage.

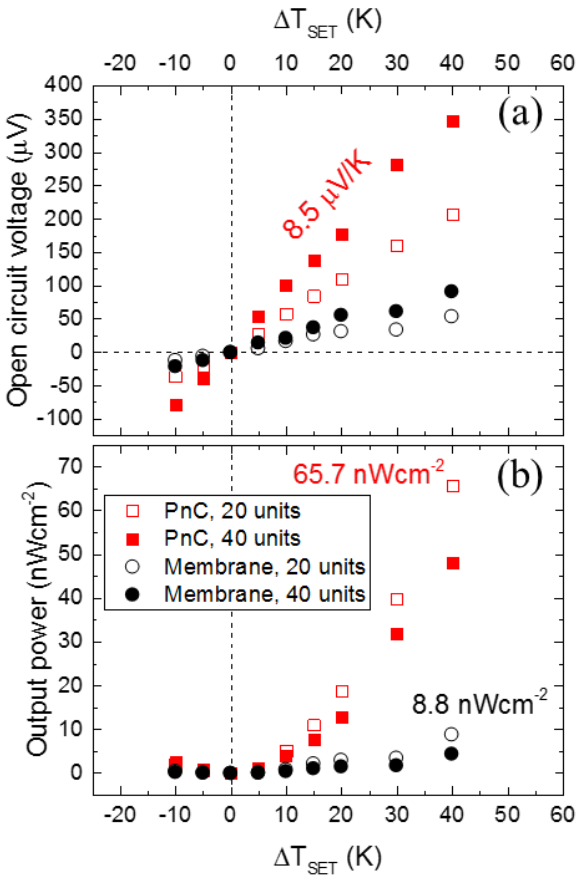

Fig. 2 (a) Measured open circuit voltage of TEG and (b) output power per unit area as a function of set temperature difference. Red square for PnC TEG, and black circle for membrane TEG.

Figure 2(b) shows that the PnC device achieves 7 times large output power. This enhancement is larger than the amount of ZT improvement in the PnC material which is about 4 times large value than membrane without PnC [5]. Although the PnCs decrease electrical properties, for the device performance, it is play more important role that large temperature difference induced by the PnC.

Output power of PnC device reached 65.7 nW from 40 K environmental temperature difference with assumption of 1 cm^2 integration, but this value is not enough for IoT sensor network. Main problem is that suspended part is not well cooled and only 1 % of temperature difference is induced in TEG from environment. Another design for the heat sink in suspended part can help further improvement for the next.

4. Conclusions

We fabricated the uni-leg TEG with PnC nanostructure and measured the thermoelectric power of TEG. We demonstrated the PnC TEG can enhance the output power more than 7 times larger than the membrane TEG. We also showed the uni-leg TEG works successfully which can be fabricated less steps compare to the traditional TEG and easily integrated with other silicon devices. For the further improvement of output power, the optimal heat sink design is required and as a result more than few μWcm^{-2} power is expected.

Acknowledgements

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