

Demonstration of a Silicon Thin Film, Phonon Engineered Thermoelectric Converter

Thierno-Moussa Bah^{1,2}, Stanislav Didenko², Stephane Monfray¹, Thomas Skotnicki¹, Frederic Boeuf¹, Emmanuel Dubois² and Jean-François Robillard²

¹ STMicroelectronics
850 rue Jean Monnet
38920 Crolles, France

² Univ. Lille, CNRS, Centrale Lille, ISEN, Univ. Valenciennes, UMR 8520 - IEMN,
F-59000 Lille, France

Phone : +33-3-20197918 E-mail : jean-francois.robillard@isen.iemn.univ-lille1.fr

Abstract

This work shows the integration of phonon engineering patterns into suspended thin silicon membranes used as a thermoelectric harvesting material. The demonstrator comprises 50 thermocouples of two silicon membranes (n and p-type) associated electrically in series and thermally in parallel. The membranes are 50 μm long, 10 μm wide and 57nm thick and patterned with 40nm diameter, 100nm pitch, hole patterns. At the center of the thermocouples, a platinum resistor is embedded to simulate the heat source. The cold side is regulated at 25°C. We report an effective Seebeck coefficient $|S_n| + S_p$ of 716 $\mu\text{V/K}$ per thermocouple and cross-sectional power densities of several W/cm^2 in good agreement with previous modeling results [1]. The thermoelectric harvested power ranges from hundreds of microwatts to milliwatts per cm^2 of footprint for temperature differences up to 46 K. Such output powers are more than enough to supply power to autonomous sensor nodes [2].

Keywords— Energy harvesting, Silicon, Phononic crystals, Thermoelectric generator

1. Introduction

The feasibility of silicon based thermoelectric generators is a topic of high interest in the thermoelectric energy harvesting community. Compared to conventional materials used for commercial thermoelectric generators such as Bi, Te and Sb, silicon holds the advantages to be the most widespread semi-conductor material, environmentally less harmful and benefits from existing facilities and processing technologies developed for low cost mass production. However, the high thermal conductivity of bulk silicon makes it a very poor thermoelectric material especially for applications close to room temperature. Hence, thermal conductivity reduction is the key to upgrade silicon as an efficient thermoelectric material. To that end, efforts are oriented towards the phononic part of heat transport, which is the dominant contribution in semiconductors [3]. This reduction can be achieved by reducing the phonon mean free path and/or the phonon group velocity e.g. by use of thin films [4], nanowires [5], addition of impurities [6] and silicon nano-patterning [7,8]. Previous works have shown that periodical hole structures, so-called phononic crystals, are able to further downscale the thermal conductivity with minor impact on the electrical conductivity [9]. The combination of the thin film and the phononic crystal enables reaching a thermal conductivity from 34 W/m/K [8] down to

as low as 2 W/m/K [7]. In this paper, we deal with the integration of phononic-engineered thin silicon membranes into a thermoelectric harvester. In the following, we present the fabrication scheme and we discuss the results of characterization of this TEG.

2. Fabrication

The demonstrator comprises 50 thermocouples electrically connected in series and thermally in parallel (Fig 1-a). It is equipped with four pads used to supply heating power and I-V measurements. Each thermocouple is composed of two n- and p-doped membranes as shown in Fig. 1-b. At the center of the platform, two platinum islands are deposited in order to electrically short the p-n boundary (Fig 1-b).

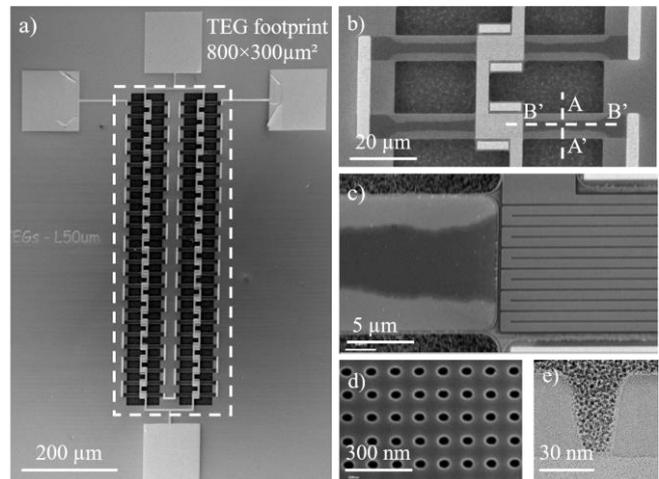


Fig. 1: Scanning Electron Micrograph of the 50 elements thermoelectric generator (a). Close-up view of two thermopile (b). Platinum resistive heater (c). Detail of the membranes phononic patterns (d). Transmission Electron Micrograph of the membrane (before suspension) (e).

An additional silicon nitride layer insulates and supports a platinum resistive heater shown on Fig 1-c used to simulate the heat sources. The membranes are patterned with a lattice of hole, called phononic crystal, which greatly increases phonon diffusion resulting in a significant reduction of thermal conductivity (Fig. 1-d). Fig. 1-e shows a Transmission Electron Microscopy cross-section of the phononic pattern before the etching of holes down to the buried oxide of a Silicon-On-Insulator (SOI) and prior to membrane suspension. The membranes are 50 μm long, 10 μm wide and 57nm thick. The ends are anchored to the silicon substrate such that heat dissipation is maximal at the

cold sides, the temperature of which is assumed to be the same as the regulated measurement plate (25°C). The measurements are realized under vacuum in order to get rid of the thermal convection in air. The hot source is simulated by Joule effect through the platinum serpentine at the center of the thermocouples (Fig 1-d) which are also used as thermometers with a thermal resistance coefficient $\alpha = 2.7 \times 10^{-3}/K$.

3. Results and Discussion

The measured dopant concentration in silicon membranes is $6 \times 10^{18}/cm^3$ for both p and n type. Heating the center of the thermocouples generates a voltage into the silicon membranes. The measured voltage drop is represented according to temperature difference across the TEG in Fig 2-a. We report from this figure, an effective Seebeck coefficient $S_{p+|Sn|}=716\mu V/K$ per thermocouple. To complete the TEG characterization, we performed an I-V characterization of the TEG at different temperature difference. The results are reported in fig 2-b. The negative $I \times V$ product is consistent with the generator regime. The open-loop voltage and the short-circuit current linearly increase with the temperature difference applied to the TEG as expected from the Seebeck effect.

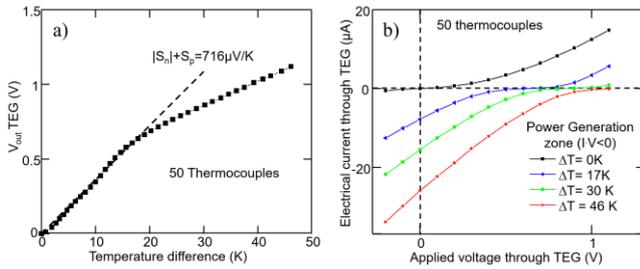


Fig. 2: output voltage versus temperature difference across the TEG (a), I-V characteristics of the TEG (b)

Fig 3-a presents the harvested power for a cm^2 footprint TEG. Remarkably, electric power up to a few mW/cm^2 can be harvested under $\Delta T=46K$, which is more than enough to power supply autonomous sensor nodes [2]. Moreover, in fig 3-b, we confirm experimentally previous modeling results [1].

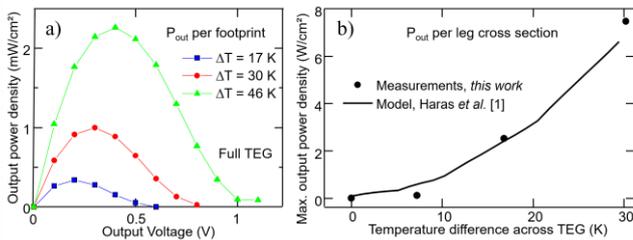


Fig. 3: Output power per TEG footprint versus the output voltage (a), Maximum output power per membrane cross-section and per thermocouple – Benchmarking with previous work (b)

Table 1 compares the harvested power per cm^2 of TEG and per thermocouple measured in this work to TEG from literature. Our TEG exhibits performance below those of the Bi_2Te_3 based TEG as this material remains a reference for room temperature applications thermoelectric harvesters. This difference can be largely compensated in use-cases where no or small heat sink is used above the thermo-

generator, as in-plane sustained Si-structures manage far better the thermal gradient compared to vertical Bi_2Te_3 pillars [13]. In addition, when our approach is benchmarked with other silicon based TEGs, we observe that it competes and even outperforms them. Indeed, polysilicon based TEG suffers from a poor electrical conductivity compared to single-crystal. Silicon nanowires (NWs) are less performant because of the small cross-section of the nanowires, thus reducing the electrical conductance.

Materials	Thermocouples	$\Delta T(K)$	P_{MAX} per thermocouple ($\mu W/cm^2$)
Bi_2Te_3 [10]	140	17	1210
Poly-Si [11]	560	31.5	0.0219
Si-NWs [12]	1	50	23
Si Thin-films This work	50	17	6.74
		46	45.2

Table 1: Comparison of the obtained results with some results from literature for different materials.

4. Conclusions

We have presented the performance of a thermoelectric generator demonstrator made of thin silicon membranes coupled with a phononic crystal. We report a Seebeck coefficient per thermocouple of $|S_{n|+S_p}=716\mu V/K$. Moreover, the demonstrator allows harvesting hundredth of $\mu W/cm^2$ to mW/cm^2 . Such harvested powers offer the possibility to use a square cm of our demonstrator to power supply autonomous sensor nodes.

Acknowledgements

This work was supported by: STMicroelectronics-IEMN common laboratory, European Research Council under the European Community's Seventh Framework Programme (FP7/2007-2013) ERC Grant Agreement no. 338179, French RENATECH network, NANO2017 program, PIA EQUIPEX LEAF ANR-11-EQPX-0025.

References

- [1] M. Haras, V. Lacatena, S. Monfray, J.-F. Robillard, T. Skotnicki, and E. Dubois, *Journal of Elec Materials*, 1–6 (2014).
- [2] R.J.M. Vullers, R. van Schaijk, I. Doms, C. Van Hoof, and R. Mertens, *Solid-State Electronics*, **53**, 684–693 (2009).
- [3] J.S. Jin, *J Mech Sci Technol*, **28**, 2287–2292 (2014).
- [4] M. Haras, V. Lacatena, F. Morini, J.-F. Robillard, S. Monfray, T. Skotnicki, and E. Dubois, *Materials Letters*, **157**, 193–196 (2015).
- [5] A.I. Boukai et al, *Nature*, **451**, 168–171 (2008).
- [6] J.-H. Lee, G.A. Galli, and J.C. Grossman, *Nano Lett.*, **8**, 3750–3754 (2008).
- [7] M. Haras, V. Lacatena, T.M. Bah, S. Didenko, J.F. Robillard, S. Monfray, T. Skotnicki, and E. Dubois, *IEEE Electron Device Letters*, **37**, 1358–1361 (2016).
- [8] J. Tang, H.-T. Wang, D.H. Lee, M. Fardy, Z. Huo, T.P. Russell, and P. Yang, *Nano Lett.*, **10**, 4279–4283 (2010).
- [9] J.-K. Yu, S. Mitrovic, D. Tham, J. Varghese, and J.R. Heath, *Nat Nano*, **5**, 718–721 (2010).
- [10] H. Bottner, ICT 2005. 24th International Conference on Thermoelectrics, 2005., (2005), pp. 1–8.
- [11] K. Ziouche et al, *Journal of Microelectromechanical Systems*, **26**, 45–47 (2017).
- [12] D. Dávila et al, *Nano Energy*, **1**, 812–819 (2012).
- [13] T.-M. Bah et al., submitted to ESSDERC 2018 (unpublished)