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Fully Aligned Via Integration for beyond 7 nm

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Abstract

Scaling of back end of the line (BEOL) nodes beyond 7 nm is severely limited by the minimum insulator thickness requirement. The conventional self-aligned via scheme suffers from the loss of critical dimensions (CD) and poor chamfer control in the non-self-aligned direction thereby compromising the maximum voltage (Vmax) requirement. Fully aligned via (FAV) approach can mitigate this Vmax issue and provide relief from Vx-Mx misalignment. FAV enables the vias to be printed larger and the subsequent benefits include a reduction in the via resistance while maximizing the via contact area. In this paper we elaborate on the key process modules related to FAV integration and review the optimization and challenges for beyond 7 nm interconnects.

1. Introduction

The pattern dimension and edge placement are the two critical factors that determine the available geometry of the interconnects while scaling the BEOL pitch to smaller dimensions. With the introduction of the self-aligned via approach around the 22 nm node, the fraction of via CD control and edge placement in comparison to the dielectric spacing has grown consistently. Increasing the dielectric spacing could mitigate this issue but the exponential increase in Cu line resistance makes it imperative to strictly control the line/space symmetry to keep the resistance low. Therefore, it is evident that lowering the technology Vmax without increasing the line resistance is key to pitch scaling.

Fully aligned via is a BEOL integration scheme where the via is self-aligned to the metal above and the metal below. The conventional trench metal hard mask is used to align the via to the metal above and a guiding topography is created to align the via with the metal below. Creation of this metal topography is unique to this FAV scheme. The advantages of this new FAV integration scheme include an increase in Vx-Mx spacing. Since the via landing dimension is confined to the metal width therefore the available minimum insulator spacing is maximized. This increase in worst case spacing can be leveraged to drive larger line/space asymmetry with reduced line resistance and decreased via resistance through the via contact area increase.

The key process modules for FAV integration are

i. guiding topography creation by metal recess
ii. high selectivity dielectric capping
iii. low-k insulator gap fill

In this paper, all these modules will be explored, and the process optimization and challenges related to beyond 7 nm will be discussed.

2. Fully Aligned Via (FAV) Integration Scheme

The process flow for FAV integration scheme is shown in Figure 1.

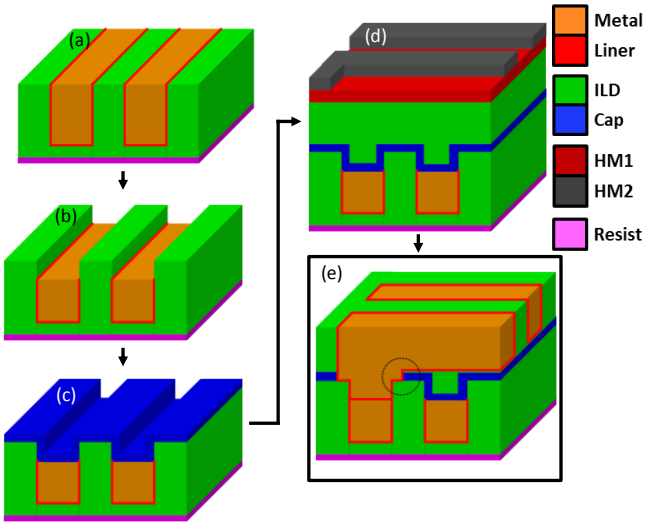

Figure1: FAV integration scheme adapted from Briggs et.al [1]: (a) Incoming profile post Mx CMP (b) Mx metal recess for topography creation (c) Deposition of conformal dielectric etch stop layer (d) Gap fill with low k dielectric (e)Vx/Mx+1 module.

3. Fully Aligned Via (FAV) modules

Mx topography creation

Creation of topography for FAV can be achieved either by recessing the wire and metal barrier or by selective insulator deposition on the inter-wire dielectric surface. The available selective insulator deposition schemes involve the usage of materials with high dielectric constant, so this option was not explored in the current study. Metal recessing was performed using a wet chemistry “A” while the TaN barrier was removed using chemistry “C” in a single wafer 300mm tool. The wet etch chemistry “A” is extremely sensitive to the incoming metal fill quality and any voids will result in large

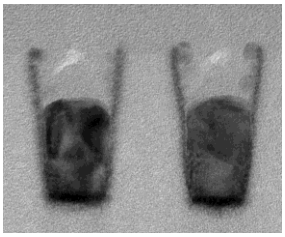

Figure 2: Cross section showing FAV topography creation by recessing Cu.

variations in Cu recess depth which will adversely affect the resistance distribution. Also, if there is a center to edge non-uniformity in trench height incoming to metal recess, there is a risk of broadening the resistance distribution further post recess. The short bath life of chemistry "C" is also one of the key challenges. Optimizations were performed to develop a wet etch strategy that takes care of both issues and lead to a flat recess profile with minimum Co divot and an average recess height of 10 nm within the specified 3σ limits [Figure 2].

Highly selective dielectric capping

The unique FAV integration and the resistance-capacitance target for beyond 7 nm requires an extreme selective etch stop layer with an etch selectivity of greater than 1:4 and a step coverage of 40% or more. The RC target requires the dielectric constant to be lower than 5 with a breakdown at 4 MV/cm and a leakage current less than 1e-7 A/ cm^2. We have developed a multilayer etch stop layer that meets all the above-mentioned criteria and can be scaled effectively to a thickness of 6 nm with a k of 4.3. This dielectric constant of the etch stop layer lowers our total capacitance by 4% while meeting high etch selectivity and EM targets [1].

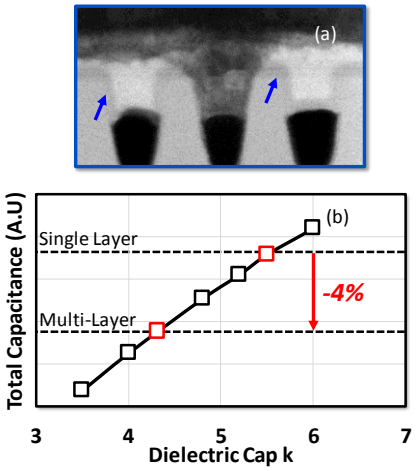

Figure 3: Conformal multilayer etch stop layer for FAV (a) Cross section showing FAV topography with the etch stop layer (b) Plot showing capacitance decrease for multi-layer films with lower dielectric constant in comparison to single layer cap.

Low-k insulator gap fill

FAV integration scheme requires 10 nm of void free gap fill. We evaluated PECVD, spin-on, dep-etch and flowable low-k films for potential gap fill application. The flowable film demonstrated excellent gap fill properties, self-planarizing ability and ease of operation. The dielectric constant of the flowable gap fill material varies from 2.7-2.8 with a breakdown of 10 MV/cm. One of the key challenges while developing this film was its high porosity which may make it susceptible to plasma induced damage during RIE processes. However, the excellent fill quality, low dielectric constant, superior electrical property, ease of operation and compatibility with the FAV integration makes it superior than the other options evaluated for FAV gap fill.

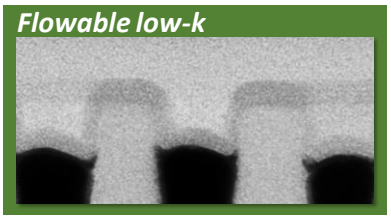

Figure 4: Cross-section of FAV gap fill with flowable low-k insulator showing void free fill

4. Comparison of FAV integration vs SAV

Figure 5 shows the clear improvement in the CD and chamfer in the FAV integration landing on Mx versus the conventional SAV flow. The SAV flow suffers from a lack of CD and chamfer control in the non-SAV direction which is mitigated by FAV.

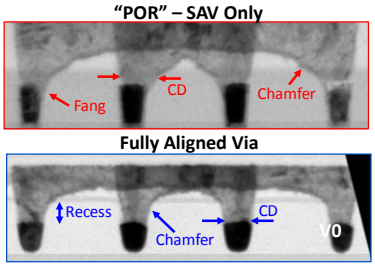

Figure 5: Cross sections comparing the SAV vs FAV integration

5. Conclusions

In this paper we discuss the FAV integration scheme, first demonstrated by Briggs et al. [1]. The unique benefits of FAV include reduction in line resistance and increase in via contact area both of which are key to scaling beyond 7 nm nodes. Implementation of this scheme also lead to high electrical yields and improvement in TDDB lifetimes [1] which are key for post 36 nm pitch BEOL interconnects.

Acknowledgements

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References

[1] BD Briggs et al." Fully aligned via integration for extendibility of interconnects to beyond the 7 nm node. "IEDM (2017)