

Title: A Moore's law for Packaging**Author : Subramanian S. Iyer****Affiliation: Center for Heterogeneous Integration and Performance Scaling (CHIPS), Henry Samueli School of Engineering and Applied Science, University of California, Los Angeles, CA 90095****Email: s.s.iyer@ucla.edu****Abstract:**

While Silicon has scaled aggressively by over a factor of a few thousand over the last six decades the progress in packaging has been more modest – a linear factor 4-5 in most cases. In this talk, we will examine the reasons for this lag and what we are doing to fix this imbalance. Packaging is undergoing a renaissance where chip-to-chip interconnects can approach the densities of on-chip interconnects. We will discuss the technologies that are making this happen and how these can change our thinking on architecture and future manufacturing. Specifically, we will discuss two embodiments: Silicon as the next generation packaging substrate, and Flexible electronics using fan-out wafer level processing. Finally, we'll discuss how these developments can help put some intelligence into Artificial Intelligence and bring about change in Medical Engineering.