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CMOS Area Scaling and the Need for High Aspect Ratio Vias

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Abstract - Resolving internal routing congestion will be essential to enable CMOS area scaling to the N5 node and beyond. The solution will require new design maneuvers in place and route (PnR), as well as patterning innovations. In this work, we present inter-layer high aspect ratio vias or 'SuperVia' (SV) as one technology element that could enable track height scaling to 4.5T at aggressive N5 dimensions. We present morphological results of the patterning scheme and discuss the impact of process variations on SV resistance obtained from empirical resistance simulations.

I. INTRODUCTION AND DESIGN MOTIVATIONS

Traditional CMOS node scaling has emphasized dimension reduction of contacted poly pitch (CPP) and interconnect metal pitch to arrive at a 50% area reduction for an equivalent node-to-node power-performance trade-off. However, continued shrinking of critical dimensions (CD) is becoming increasingly challenging due to device electrostatic limitations associated with channel control in the FEOL and RC increase in the BEOL. Hence, there is increasing interest to explore alternative approaches to area scaling, one of which is track height reduction in logic standard cell. It has been demonstrated, using N5 design rules (Table 1), that scaling the track height from 6.5T to 4.5T, can produce an area gain of more than 30% [1]. However, internal routing within a 4.5T cell becomes challenging due to congestion brought about by the presence of transition metal pads (minMetal) in the intermediate metal layer. As a direct response to this problem, we propose to replace, where possible, minMetal instances with high aspect ratio SV. The associated benefits include routing decongestion, more efficient utilization of routing resources, and potential track height reduction, as illustrated in Fig.1. By definition, a SV is a via that provides direct connection from, say, M_{x+2} to M_x metal layer, by-passing the intermediate layer M_{x+1}.

II. INTEGRATION PROCESS FLOW

Patterning of the SV follows M_{x+2} trench transfer into TiN in a trench-first-metal-hardmask (TFMH) scheme. A tri-layer coating consisting of spin-on carbon (SoC), spin-on-glass (SoG) and photoresist is then processed, followed by the SV lithography which can be done either by EUV or 193i. High-aspect-ratio (AR>13) dry etch is then used to transfer the SV patterns through a multilayer stack consisting of organic and dielectric materials. In the next step, a thin conformal isolation barrier is deposited, after which spacer-like directional etch is applied to expose the metal at the via bottom. For the metal fill of the SV, a selective bottom-up deposition process is proposed, where the height of the SV is only partially filled. The metal of choice can be Cu, Co, or Ru, using substrate-selective deposition techniques demonstrated in [2-5] Fig. 3 shows morphological results of the SV patterning and metal fill using electro-less deposition of Cobalt. The remaining steps of the integration flow is as follows; V_{x+2} lithography is followed by dual-damascene patterning creating the connection between M_{x+2} and M_{x+1}; TiN wet strip; metallization and CMP.

III. EXPERIMENTAL RESULTS AND DISCUSSION

N5 process assumptions shown in Table 2. were used to simulate a three-level interconnect configuration using Coventor SEMulator3D®, and resistance and capacitance (RC) extractions were performed using the software integrated solvers. These solvers employ standard volume discretization methods to solve the underlying Laplace equation for both resistance and capacitance,

$$\nabla \cdot (\sigma \nabla \varphi) = 0, \qquad \nabla \cdot (\varepsilon \nabla \varphi) = 0$$

where φ is the electric potential, ε is the dielectric permittivity for capacitance extraction, and σ is the electrical conductivity for resistance extraction. In Fig. 4, SV resistance is compared, at equivalent via cross-sectional area, to the resistance of a regular stacked via running from M1 to M3 through minMetal in M2. The SV resistance is 40% lower because of the presence of only one barrier/liner (B/L) interface as compared to two B/L interfaces present in the stacked via scenario. Due to the removal of some minMetal in the intermediate M2 layer for SV implementation, a 10% capacitance reduction between two parallel M3 wires is observed in the simple device layout we used for the model simulation, as shown in Fig. 5. At a system level, the absolute capacitance benefit derivable is design specific and proportional to the density of SV deployed to replace stacked vias. One of the main challenges of a selective deposition process for via fill applications is a height non-uniformity of the grown metal. To understand the impact of SV metal height variability on resistance, height ranges from 10 to 100nm for Co SV in combination with TaNRu B/L are shown in Fig. 6. For wide SV cross-sectional area, there is a resistance variability of up to 50% for a 10-fold increase in SV metal height. Also, by increasing the metal height, there is a significant drop in resistance which can be attributed to the increase in contact area at the point where M3 metallization meets the SV. This trend is consistent with a solution of the resistance equation $R = \rho L/A$ for all participating resistors in series, (where ρ is the metal bulk resistivity, L is the length of the conductor, and A is the area). This reduction of resistance is more pronounced in the case of very small SV area where up to 80% resistance decrease can be obtained. Figs. 7-9 presents the simulated resistance trends when Co, Cu or Ru SV are combined with MnRu, TaNCo, or TaNRu B/Ls at M3. For this illustration, a total B/L thickness of 3nm is assumed with 2nm TaN and 1nm Co or Ru liner. It is observed that for Co or Cu SV metal in combination with TaN-based B/L scheme, there is a constant reduction in SV resistance with increasing SV metal height. This is because the ratio to total resistance contributed by the high resistive M3 metal interface decreases at a faster rate than the resistance increase of the low resistive Cu and Co SVs. MnRu M3 B/L, on the other hand, show the opposite trend with respect to SV height, due to its lower resistivity, making the increase in SV height result in increased total resistance. The impact of SV overlay on resistance and SV isolation to neighboring M2 was also studied. Fig. 10 shows that increasing the dielectric liner thickness results in larger SV to M2 isolation distance, which will lower metal-to-metal coupling capacitance. However, contact area reduces with increased dielectric liner, with a consequent resistance increase. Due to the self-alignment of the SV, an inverse proportional relationship between overlay shift in one direction and SV contact area is observed as shown in Fig. 11. For a via placed at zero extension to M3, a SV area reduction is to be expected only when the overlay shift causes the SV to overlap on the metal hardmask, otherwise SV area should remain unchanged as is the case in the positive overlay region in Fig. 11.

IV. CONCLUSIONS

High aspect ratio SuperVia is introduced as a scaling booster, with the potential to enable track height scaling to 4.5T using N5 design rules. Patterning feasibility of SV was demonstrated using a dual-damascene-compatible self-aligned integration scheme promising lower access resistance compared to traditional damascene multi-via stack. Electrical extractions performed using Coventor SEMulator3D® integrated solver show 40% resistance and 10% capacitance advantage in favor of SV over regular stacked vias.

REFERENCES

[1] S. M. Y. Sherazi, et. al., "Track height reduction for standard-cell in below 5nm node: How low can you go?", SPIE 2018; [2] K. Vandersmissen, et. al., "Demonstration of a cost effective Cu electroless TSV metallization scheme", IITC 2015; [3] M. H. van der Veen, et.al., "Cobalt bottom-up contact and via prefill enabling advanced logic and DRAM technologies", IITC 2015; [4] Y. Jiang, et. al., "Development of electroless Co via-prefill to enable advanced BeOL metallization and via resistance reduction", IITC 2016; [5] J. Goswami, et. al. (2005), "Selective deposition of ruthenium films by digital CVD". Chemical Vapor Deposition, 11(2), 94-98. DOI: 10.1002/cvde.200304176;

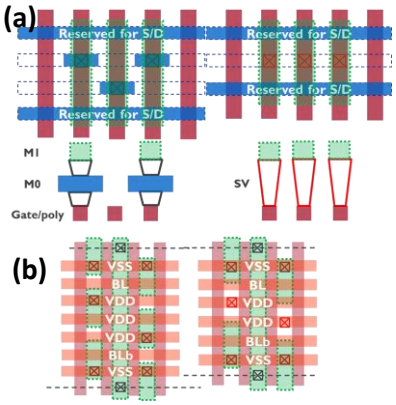

Fig. 1: SV eliminate routing congestion and enable standard cell track height scaling to 4T (a) direct M1 to gate contact makes it possible to arrange pins on a single track (b) in SRAM, M2 to M0 contact with SV can relax T2T and minMetal rules in M1

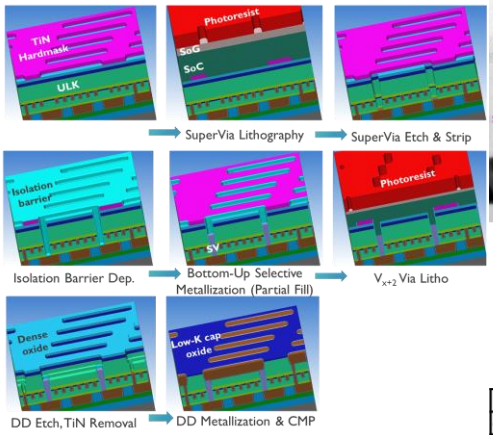

Fig. 2: Self-aligned HAR SuperVia process flow. SV is self-aligned to TiN hardmask, and SV barrier-less metallization lowers contact resistance

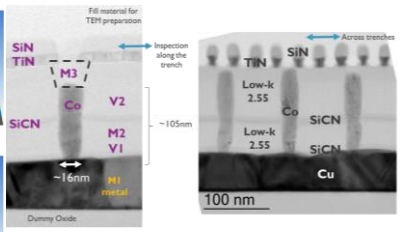

Fig. 3: XTEM showing HAR SV etched into ULK 2.55, and filled with cobalt using selective electro-less deposition process. Bottom-up fill process not sensitive to HAR and via profile.

Table 1: iN5 Design Rules

Layer	CD(nm)	Pitch(nm)
Gate	18	42
M_{int}	10.5	21
M_{int} Block/t2t	18	-
M1	10.5	21
SV	10.5	42

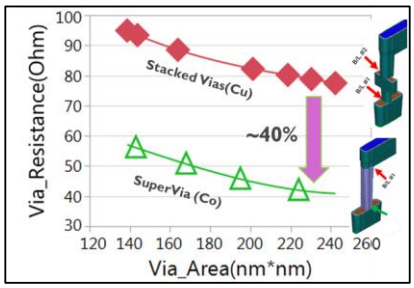

Fig. 4: Simulated resistance of SV vs. stacked vias. SV metal: Co, M3 B/L: 2nm TaN/1nm Ru

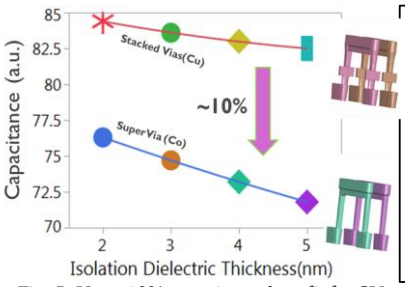

Fig. 5: Up to 10% capacitance benefit for SV due to elimination of minMetal in M2. Increase isolation dielectric reduces capacitance, but leads to resistance penalty

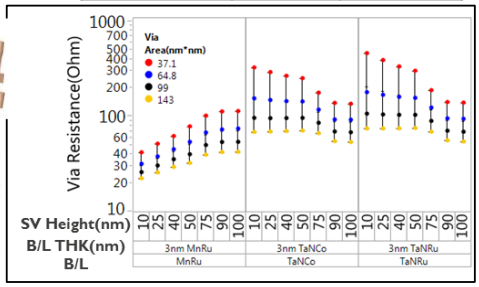

Fig. 7: Co SuperVia: impact of barrier liner material type on SV resistance

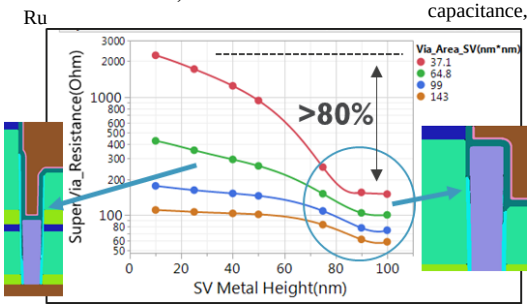

Fig. 6: Impact of SV metal height and contact area on SV resistance. At smaller via area, increasing Co height into the M3 can reduce via resistance significantly due to larger M3 to SV contact surface. SV metal: Co, M3 B/L: 2nm TaN/ 1nm Ru

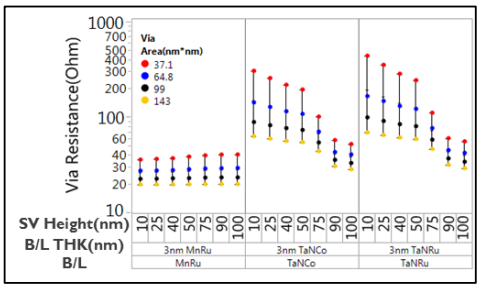

Fig. 8: Cu SuperVia : impact of barrier liner material type on SV resistance

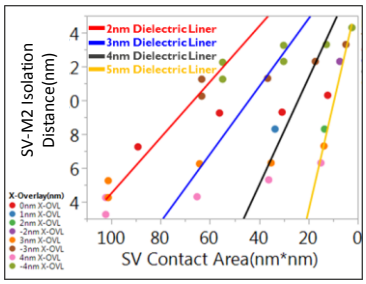

Fig. 10: SV-M2 isolation distance and SV contact area as a function of dielectric liner thickness and SV overlay. Liner thickness indirectly proportional to SV contact area, directly proportional to SV-M2 isolation distance.

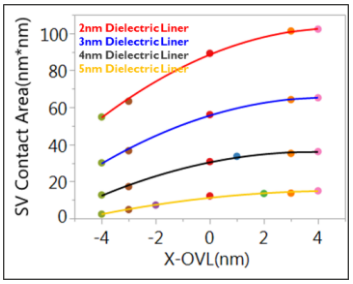

Fig. 11: SV overlay impact on SV contact area. SV overlay shift in the negative X-direction leads to contact area decrease, while a shift in positive X-direction should not impact SV area

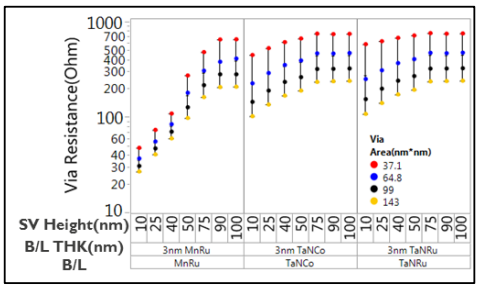

Fig. 9: Ru SuperVia : impact of barrier liner material type on SV resistance

Table 2: Design Rules Used for Electrical Simulation

Layer	CD(nm)	Pitch(nm)	Patterning
M0	18	36	EUV SE
M1	10.5	21	193i SAQP
M2	18	36	EUV SE
SV	18	-	193i