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Growth of Multi-Layer Graphene (MLG) Inside Si Deep Trench for 3D-LSI Application

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Abstract

We report the formation of multilayer graphene (MLG) along the side wall of the deep Si trenches or through Si via (TSV) that can be used for the heat removal in the stacked 3D-ICs/LSIs. Laser micro-Raman data revealed that the as-grown graphene on the flat surface of the LSI chip containing TSVs is comprised of MLG with G to D peak ratio of 1.4. However, the G/D ratio depends on the quality and thickness of Ni along the sidewall and bottom of TSV. Such graphene-TSVs formation with diameter varying from 3 μm to 20 μm and depth 30 μm to 100 μm fabricated using current-enhanced chemical vapor deposition method reveal the possibility of these graphene-TSVs as thermal management material in stacked 3D-LSIs/ICs.

Keywords: Current-enhanced CVD, MLG, TSV

1. Introduction

In 3D-LSI, several chips are staked vertically and connected by through-Si-via (TSV) in the Z-direction. By using TSV interconnections, one develop high-density wide-bandwidth chip systems with better performance at low power consumption. In addition to several process related difficulties, there is a severe reliability issue, namely heat accumulation. Hence, thermal management in 3D-LSI is very important (1). It is owing to a very large thermal conductivity of Si in parallel to the chip surface and hence the parallel conduction of heat (2). Since the chip sizes are reduced in order to have smaller form factor, the parallel heat spreading effect is highly suppressed by the very thin chips of 3D-LSI/IC and leading to hot spot. In order to solve the hot spot problem, it is generally incorporation of thermal TSV is carried out (3). Cu is generally used as TSV metal since it has very low electrical resistivity 1.7μΩ.cm and reasonable thermal conductivity ~290 W/mK.

However, an extremely high thermal conductivity value in the range of ~ 3080–5150W⁄mK (which is an order of magnitude higher than Cu) and phonon mean free path of ~ 775nm~ 775nm near room temperature were extracted for a set of graphene flakes from the micro-Raman data (4). Such high thermal conductivity value suggest graphene's applications as heat removal material in the future 3D-LSI/ICs. Hence, in this work we have attempted to grow multi-layer graphene (MLG) inside the TSV for the thermal management applications in 3D-LSIs/ICs.

2. Experimental

Fig. 1 reveals the schematic process flow for the formation of MLG inside the TSVs. The diameter and the depth of the TSVs are respectively 3 μm to 20 μm and 30 μm to 100 μm. The details regarding the current-enhanced CVD for the growth of MLG is found elsewhere (5). MLG growth period is 10 min, and the growth temperature is ~500 ℃. As grown MLGs were analyzed for their morphology using AFM, OM, SEM, EDX, and micro-Raman spectroscopy.

3. Results and Discussion

Shown fig. 2 and 3 are the optical (OM) and scanning electron microscope (SEM) images obtained for MLG grown on LSI chip with thermal TSVs. It reveals that the as-grown MLG are smooth enough and formed deep inside the TSV. The EDX 2D-mapping (fig. 4(a)) and line analysis data (fig. 4(b)) shows the formation of MLG inside the TSVs. Finally we have analyzed the quality of MLG by micro-Raman spectroscopy and the results are shown in fig. 5. The peaks around 1350 cm^{-1} and 1580 cm^{-1} are belongs to defective (D) and normal graphitic structures (G) respectively. The G/D peak ratio obtained for the MLG grown on LSI chips with thermal TSVs is 1.4, and it can be improved by current-enhanced CVD whose G/D ratio is ~6 (5). The observation of Raman peak around 2700 cm^{-1} which also clearly indicates the graphene film grown on LSI chip containing TSVs are of MLG in nature.

In summary, we were able to grow MLG inside the 20 μm-width, 100μm-deep TSV using current enhanced thermal CVD at ~500 ℃ for thermal TSV application in 3D-LSI/ICs. It is expected that the higher quality MLG will be formed inside the TSVs with further process optimization.

References: (1)S.K. Lim, IEEE Des. Test Comput. 22 (6), 532 (2005); (2)G. Luo et al, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.32(4), 510 (2013); (3) J. Fu et al, 12th IEEE Inernational Conf. on Solid-State and Integ. Circuit, 2014; (4) S. Chen et al, Nature Materials, DOI:10.1038/NMAT3207; (5) L. Razak et al, Microelectronic Engineering, 120, 200 (2014).

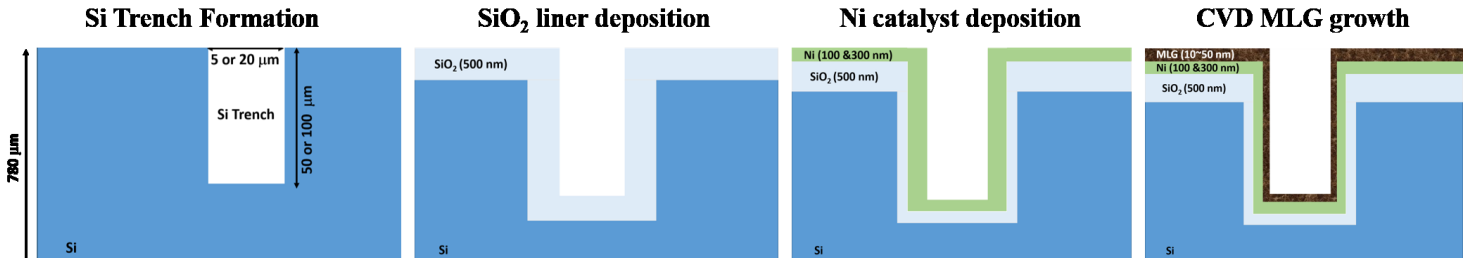

Fig. 1: Schematic process flow diagram for the growth of MLG along the sidewall of deep Si-trench by current/thermal CVD.

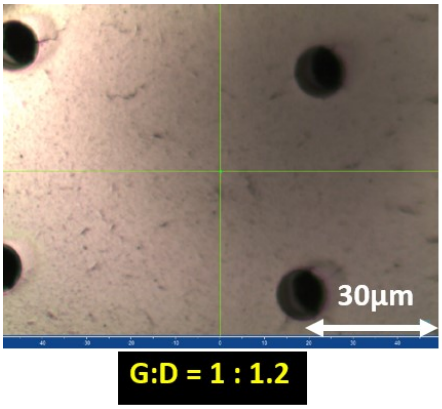

Fig. 2: Top view optical microscopic images taken after MLG growth inside the Si deep trenches on LSI chip.

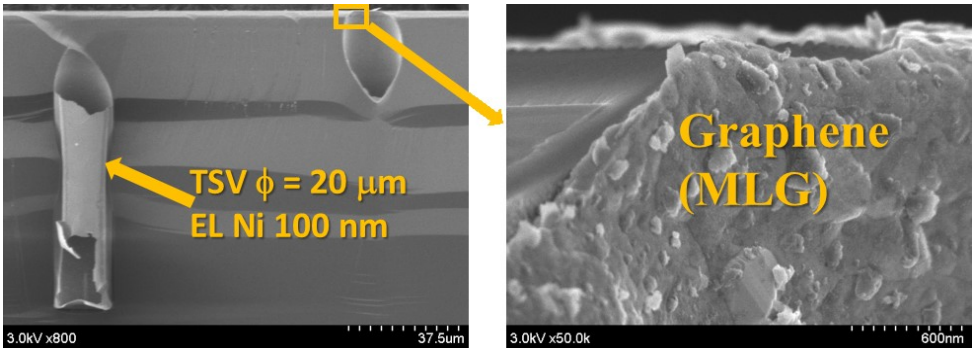

Fig. 3: X-sec. SEM images obtained for Si deep trench in LSI chip with MLG along the side wall.

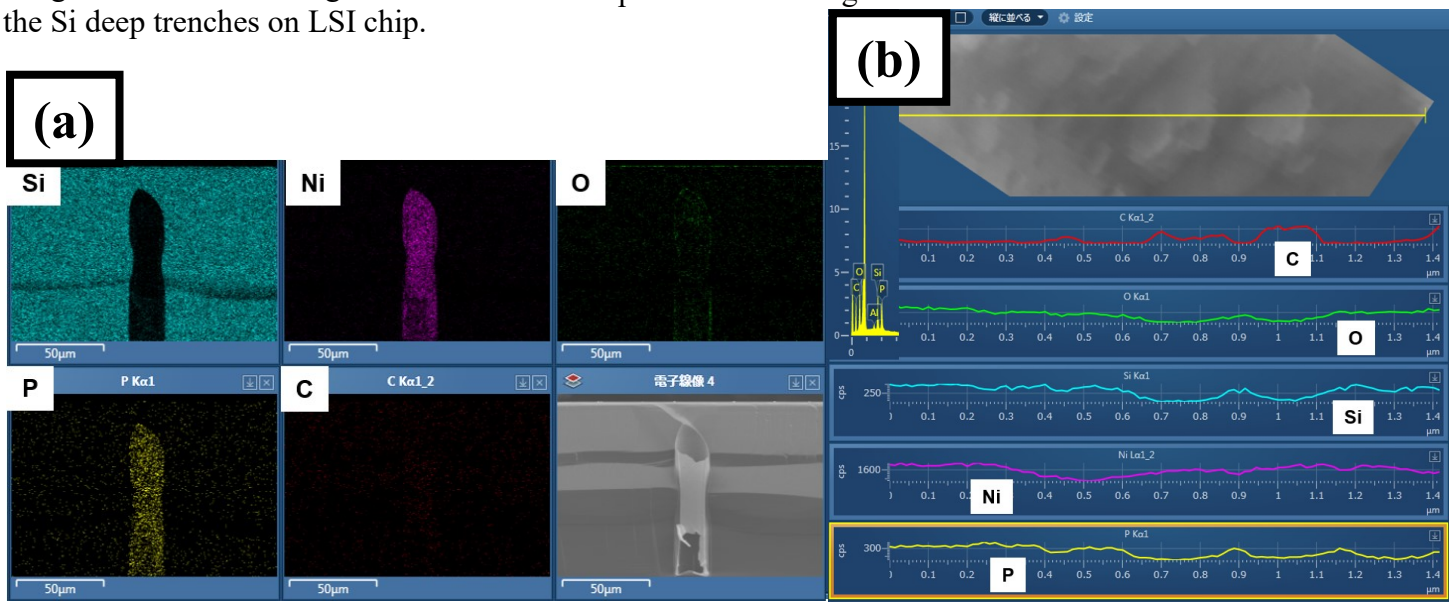

Fig. 4: EDX analysis results obtained for the cross-sectional Si trenches with MLG; (a) 2D-mapping and (b) line analysis.

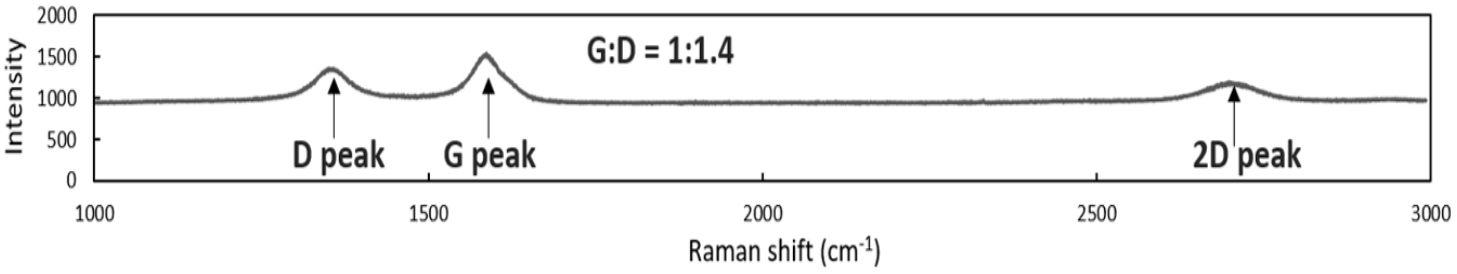

Fig. 5: Raman Spectra revealing the formation of MLG in LSI chip with thermal TSVs.