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Conductor trends for future interconnects

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Abstract

Interconnect trends along with possible future scenarios will be detailed. First, use cases of EUV patterning to interconnects in logic will be illustrated. As alternative metals are of interest to both logic and memory applications, potential conductor scenarios will also be discussed. Finally, some examples for implementation will be covered.

1. Introduction

Interconnects distribute clock and other signals, provide power and ground for various components of an electronic system. Figures of merit include speed (delay), power dissipation, noise (e.g. cross-talk), bandwidth density and reliability. To ensure power, performance, area and cost benefits back-end-of-line (BEOL) dimensional, material scaling along with innovations at the circuit level and the introduction of scaling boosters are important.

2. Multi-patterning dual damascene copper

In order to reach the dimensions required, multi-patterning dual damascene interconnects are prevalent [1-3]. The introduction of EUV patterning for BEOL holds the promise of potentially simplifying the multi-patterning requirements. Fig.1 shows 32nm metal pitch interconnects, where EUV was used either for printing blocks and vias or printing unidirectional metal lines. Fig.2 illustrates such copper interconnects after dual damascene integration. Although full immersion implementation is technically also feasible, the number of process steps requiring to realize such interconnects is substantially higher. Fig. 3 compares the number of steps needed for fabricating 3 dual damascene metal levels only with immersion lithography, hybrid EUV and full EUV. In the case of the all-immersion version 7 masking layers (1 for gratings, 3 for block and 3 for via) are necessary for dual damascene. For the hybrid EUV case 3 masking layers (immersion gratings, EUV block and via) are needed, while for the single print EUV case 2 masking layers (1 for metal lines and 1 for via) are required. The simplification of dual damascene integration along with module cost reduction are apparent.

The dimensional scaling is accompanied with track height reduction in order to reduce chip area. From an interconnect perspective it is important to point out that in such a scenario the relative importance of local (Mx) wires and vias is critical. Indeed, as shown if Fig. 4 through the example of D4 strength inverter, the Mx wire and via resistance contribution is very significant to propagation time.

2. Alternative conductors

As dimensions scale to 8nm half pitch and beyond maintaining conductor resistance and reliability requirement is increasingly difficult [3-8].

This prompts a scenario whereby the local Mx copper wires and vias are gradually replaced by alternative conductors (Fig. 5). Resistance in scaled dimensions is determined by the figure of merit $\rho_0 x \lambda$, where ρ_0 is the bulk resistivity and λ is the electron mean free path. Besides resistance requirements, reliability need to be met, for which the cohesion energy can be used as a proxy (Fig. 6). Based on such an approach a short list of alternative conductors (e.g. Rh, Pt, Ir, Ni, Co, Ru, Mo, Cr) can be established. Beyond pure elements, ternary compounds remain an interesting area for research. Fig. 7 shows experimental data illustrating that indeed Rh and Ir presents the lowest resistivity in sub-100nm^2 interconnects [5]. However, next to resistivity requirements it is also important to consider manufacturability and cost aspects. Fig. 8 shows a benchmark plot for Cu, Co and Ru in damascene wires. Below about 12nm critical dimension barrierless alternatives outperform copper. Furthermore, via resistance is the most important factor in selecting alternatives (Fig.9). Indeed, ruthenium presents the lowest via resistance followed by cobalt and copper. When introducing alternatives at the via level there might be a concern on stress induced voiding [8], as the stress gradients along the via filled with alternatives can be higher than for copper (Fig.10). Besides stress induced phenomena current carrying capabilities are critical. Fig.11 shows the fuse current benchmark for different scaled conductors and based on these the following ranking is established: Al < Cu < Co < graphene < Ru.

For using alternative metals in context, one interesting future option is related to the so-called buried rail [9], where the power rails, which are usually found in M1 layers, are rather placed below the level of fins in order to free up routing resources for interconnects (Fig.12). In such a scenario the required temperature budget is different than in BEOL, so it is critical to use metals that withstand high temperature. In Fig.13 resistivity of high aspect ratio buried ruthenium lines are shown after 650ºC and 1000ºC anneal. After high temperature treatment 33% resistivity drop is found, which is very attractive. It is a result of significant grain growth as evidenced by the cross-sectional TEM along the lines (Fig.14). Another interesting implementation option is the use of metal patterning [10]. An experimental example of such an implementation is shown in Fig.15, where single print EUV was combined with metal patterning and reproducible metal lines across the 300mm wafer were demonstrated. Combining these alternative conductors with airgaps may provide a path towards future low RC interconnects.

3. Conclusions

Interconnect trends with advanced patterning techniques, potential future scaling scenarios and implementation examples were discussed.

References

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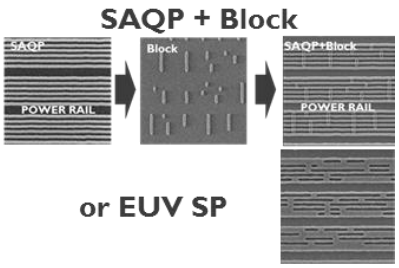

Fig.1 Example of SAQP+Block patterning vs. single print EUV option

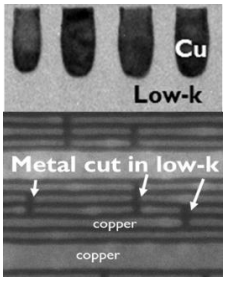

Fig.2 Cross section of SAQP copper dual damascene and top-down after CMP

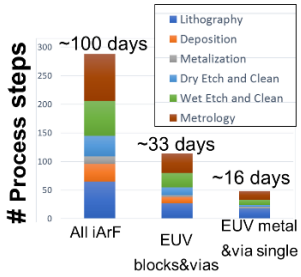

Fig.3 Process flow length with all immersion vs. EUV hybrid and full EUV

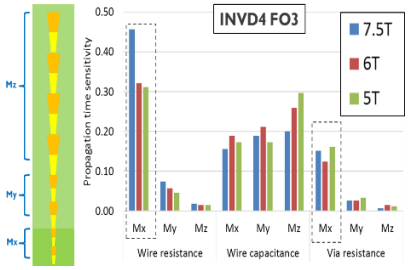

Fig.4 Relative importance of Mx wire and via (lower interconnect levels) resistance in a simple circuit with track height scaling

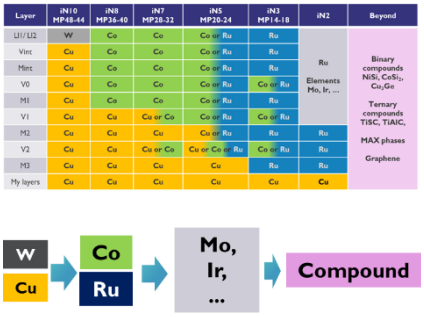

Fig.5 Introduction of alternative conductors at the different metallization levels.

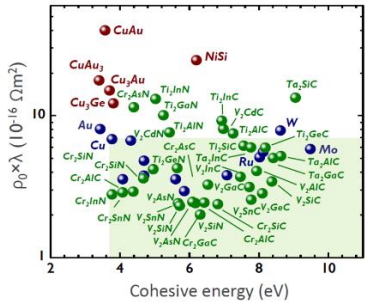

Fig.6 Figure of merit for pure elements and selected ternary compounds

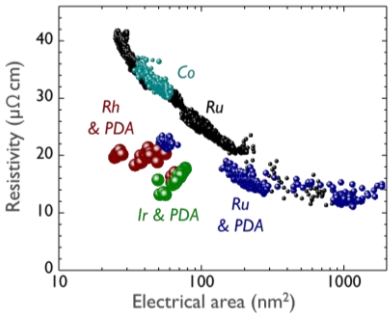

Fig.7 Experimental resistivity of Co, Ru, Ir, Rh in scaled dimensions

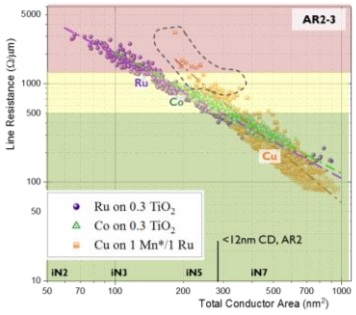

Fig.8 Cu, Co, Ru resistance benchmark in narrow lines

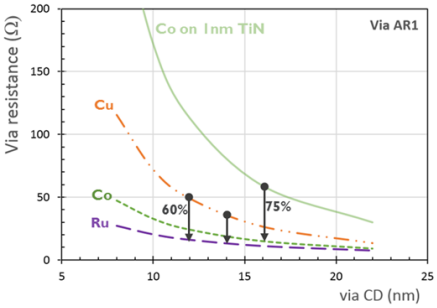

Fig.9 via resistance for Ru, Co, Cu

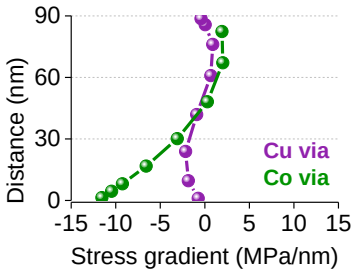

Fig.10 Stress gradient in Cu and Co vias

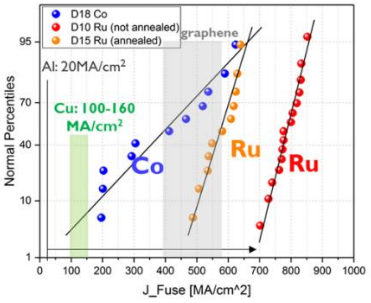

Fig.11 J_{Fuse} for Al, Cu, Co, graphene, Ru

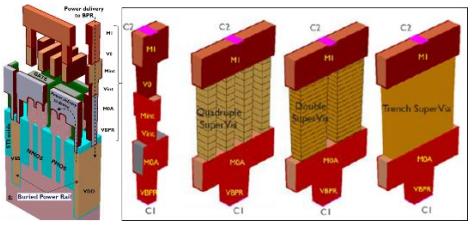

Fig.12 Concept of buried rail in combination with different C2 tapping schemes

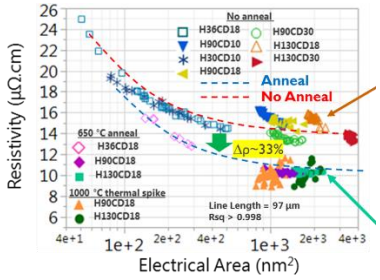

Fig.13 Resistivity of HAR Ru lines before and after high temperature anneal

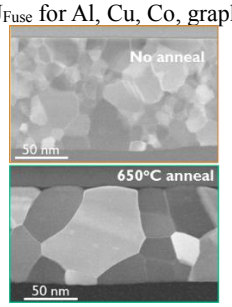

Fig.14 Grain size of Ru before and after anneal. X-TEM taken along the line.

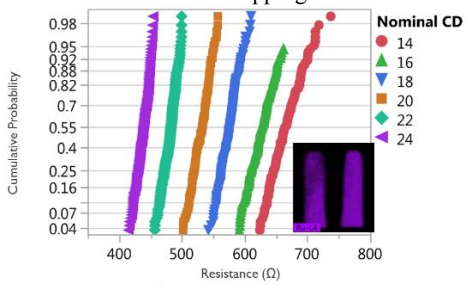

Fig.15 Line resistance of metal patterned Ru