

Implementation of a Monolithic Three-Axis Accelerometer Using an Improved CMOS MEMS Process

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Abstract

This paper presents a monolithic three-axis accelerometer fabricated using an improved complementary-metal-oxide-semiconductor (CMOS) microelectromechanical system (MEMS) process. Following the standard 0.18 μm 1P6M CMOS process, a 0.5- μm -thick amorphous silicon and a 0.6- μm -thick aluminum layer are deposited and patterned as etch-resistant masks. The masking aluminum and amorphous silicon layers are exhausted during the oxide etching and silicon-releasing process. Therefore, an amorphous silicon layer is utilized to avoid over-etching of the oxide layers in the microstructure and ensure a consistent thickness across the whole sensor device. The sensitivities of the three-axis accelerometer were determined to be 131, 130 and 85 mV/G for the x-, y- and z-axis accelerometer, respectively.

1. Introduction

Integrated accelerometers based on complementary-metal-oxide-semiconductor (CMOS) microelectromechanical systems (MEMS) technologies have been widely proposed in the last two decades. Some studies are based on the use of additional thin film deposition or bonding-wafer technology [1–2], whereas other studies typically use a standard CMOS process followed by a post-CMOS process to integrate the sensor/actuator device and readout circuits to reduce the impact of front-end CMOS process [3].

The present paper proposes a monolithic three-axis accelerometer that utilizes a 0.18 μm 1P6M improved CMOS MEMS process. Three individual sensor devices are designed and fabricated to decrease both the structural size and the bending deformation due to composite CMOS structures [4]. The sensing circuit utilizes a switched-capacitor integrator to sense capacitance changes and a trimming technique to eliminate the output DC offset voltage.

2. Improved CMOS MEMS Process

In our previous study [4], a microstructure was fabricated via the post-CMOS MEMS process using only a 0.8- μm -thick aluminum layer as the etch-resistant mask during the oxide and silicon etch. However, the underlying oxide layer in the microstructure may be over-etched when the thick aluminum layer is exhausted during the post-CMOS oxide etching (Fig. 1). To avoid over-etching the microstructure, a 0.5- μm -thick amorphous silicon layer was additionally deposited and patterned prior to the alumi-

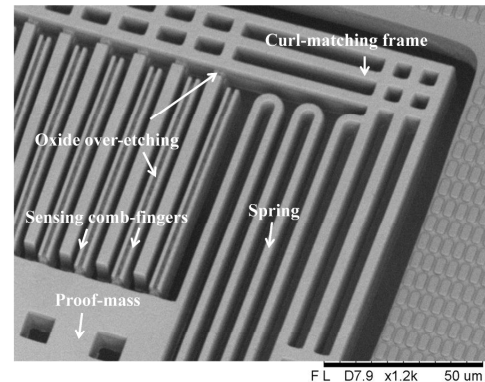


Fig. 1 CMOS MEMS comb-fingers with over-etching in oxide layers

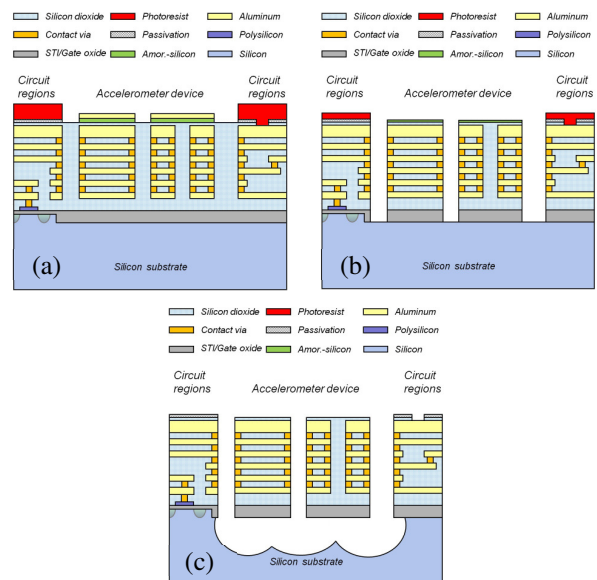


Fig. 2 Steps of improved CMOS MEMS process flow: (a) etch-resistant layers deposition and patterning, (b) anisotropic dry oxide etching, (c) isotropic dry silicon releasing.

num etch-resistant layer.

Figure 2 shows the process flow of the improved 0.18 μm CMOS MEMS process wherein following the standard CMOS process, a dioxide layer, an amorphous silicon layer, and an aluminum layer are sequentially deposited on the top metal layer (metal-6 layer in this case) as an etch-resistant mask. Next, the CMOS passivation layers are deposited and patterned except for the sensor device region. Following this, a 12- μm -thick photoresist layer is defined above the circuit region for etch protection. The post-CMOS

micromachining is performed using inductively coupled plasma with CF_4 and C_4F_8 to anisotropically etch the oxide between structural sidewalls. The $0.5\text{-}\mu\text{m}$ -thick amorphous silicon layer can effectively protect the oxide layer from being over-etched and ensures a consistent microstructure thickness. The microstructure is then released via an isotropic silicon undercut etch using SF_6 . The wafer is finally cleaned using an O_2 plasma to ensure the removal of the photoresist layer. The sensor device thickness is up to $10.3\text{ }\mu\text{m}$, which is derived from the thickness of the CMOS layers. The minimum gap spacing between the microstructure is $2\text{ }\mu\text{m}$.

3. Design and Experimental Results

The x- and y-axis accelerometers both comprise four mechanical springs with a proof-mass. Comb-fingers are attached to the proof-mass to form the sensing electrodes. A curl-matching frame is placed around the device to compensate the coupling mismatch from comb-fingers of rotors and stators, which is due to the stress gradient in stacked CMOS layers. The z-axis accelerometer employs the torsional beam and asymmetric proof-mass with comb-fingers.

A switched-capacitor circuit with a trimming mechanism is used to sense the capacitance changes in Fig. 3. The first stage converts capacitance to voltage with a gain of approximately $2\Delta C/C_{\text{int}}$, where C_{int} is about 200 fF , and ΔC is the capacitance change. An external 8-bit trimming pattern is added to a digital to analog converter that generates a reverse offset current to the input-node of the pre-amp to compensate the output offset voltage due to the sensing gap mismatch in comb-fingers.

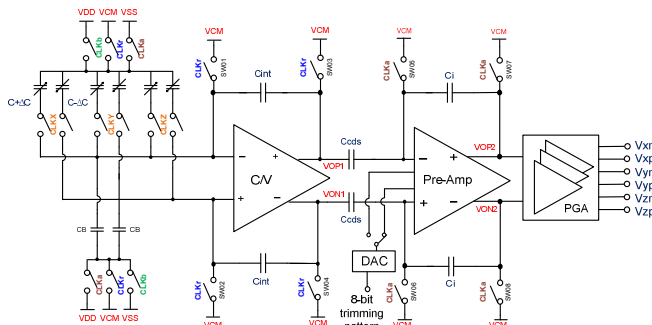


Fig. 3 Schematic of switched-capacitor sensing circuits with trimming diagram

Figure 4 shows the scanning electron microscope (SEM) image of the three-axis monolithic accelerometer fabricated using the improved CMOS MEMS process. The oxide over-etching issues at the comb-fingers side have been addressed to produce a consistent microstructure thickness, which is achieved using an amorphous silicon layer (Fig. 5.) Filled oxide layers in the microstructure can protect narrow CMOS metal electrodes from peeling off when the accelerometer is under shock excitation. Figure 6 shows the output sensitivities of the three-axis accelerometer, where are 131, 130 and 85 mV/G across the range of $0\text{--}6\text{ G}$ for the x-, y- and z-axis accelerometer, respectively.

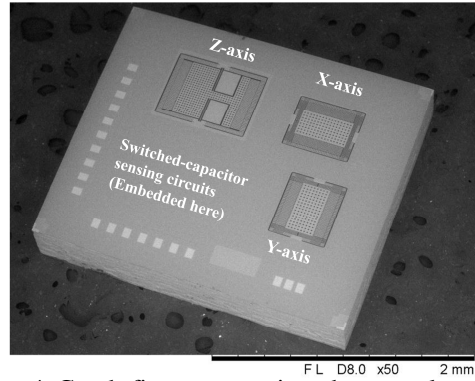


Fig. 4 Comb-fingers covering the complete oxide layer due to the protection of the amorphous layer.

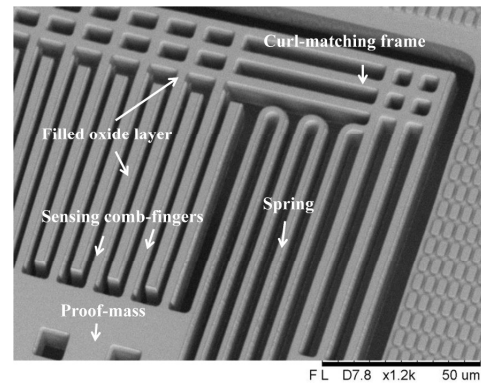


Fig. 5 Comb-fingers covering the complete oxide layer due to the protection of the amorphous layer.

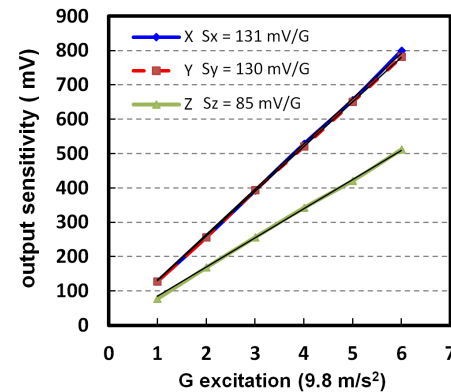


Fig. 6 Sensitivities of the three-axis accelerometer

4. Conclusions

This paper proposes a monolithic three-axis accelerometer using an improved CMOS MEMS process. By integrating with CMOS process, it can be directly applied to the circuit system as an embedded sensing unit.

Acknowledgements

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References

- [1] A. E. Franke *et al*, *IEEE MEMS Conf.* (1999) 630.
- [2] S. L. Chua *et al*, *IEEE VLSI Symp.* (2014) 978.
- [3] H. Sun *et al*, *IEEE J. Sensors* **11** (2011) 925.
- [4] S. H. Tseng *et al*, *J. Micromech. and Microeng.* **22** (2012).