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Evaluation of Advanced Process Integration Options for next Generation of Si-Photonics platform

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***Abstract* – Advanced process integration options on a 300mm Si-Photonics platform are proposed. Impact of immersion lithography, multi-Si etching and integration of a 3D SiN waveguide layer are discussed.**

1. Introduction

Silicon Photonics has received a growing interest due to its low cost, allowing this technology to enter the datacenters. Few years ago we demonstrated the manufacturability of a 300mm wafer based Si-photonics process [1] for 100G-PSM4 applications. Recently the definition of 200G and 400G standards showed the need for devices able to withstand lower link budget (lower insertion loss), higher modulation order, such as PAM-4, along with CWDM support. These new challenges can be achieved by a proper device design but are also relying on some process improvement. With respect to our previous technological platform, we propose here to assess different integration schemes such as (i) the integration of multiple waveguide types: strip and rib with various slab thicknesses, (ii) the introduction of immersion lithography to improve process control, and (iii) the introduction of an additional 3D waveguide layer of SiN waveguides above the standard Si layer.

2. Multiple Patterning

To extend the application range of Si-photonic platforms, optical device designers needs to be able to access to a wide range of n_{eff} values. In some cases, the simple change of the waveguide width is not enough and the introduction of various waveguide types is mandatory. Starting from a 310nm SOI thickness, we introduced a multiple and self-aligned patterning scheme to define rib waveguide with 165nm slab thickness (rib), rib waveguide with 50nm slab thickness (deep-rib) and strip-waveguides. After a TEOS/SiN hardmask deposition, a first 193nm lithography and a first Si-RIE are performed to define the top of all the waveguide type and a 165nm slab level on the whole wafer. Then two other patterning levels are used to further etch the slab to form the deep-rib and strip waveguides, using the TEOS/SiN hardmask for self-alignment with the first lithography step. One of the challenge is to keep a low dispersion of the remaining Si-thickness in rib and deep-rib waveguides due to the multiple etching sequence. After optimization, the measured of remaining Si-thickness values shows a within wafer range of 4.2 nm and 7 nm for rib and deep-rib etching respectively. Measured single mode waveguide losses are 1.6dB/cm on W=0.4µm Rib waveguides, 2.6 dB/cm on W=0.45µm deep-rib waveguides and 5.6 dB/cm on W= 0.35 µm strip-waveguides. If the 165nm etching process is key to optimize the performance of grating couplers, the use of deep-rib waveguides enables new devices, such as 5 to 10µm bend-radii ring resonators co-integration (fig.1b). Since deep-rib waveguide improves the mode confinement into the ridge it can also be used to improve the overlap between the optical mode and a PN junction depletion zone to fabricate improved phase shifters (fig. 2). Linear phase shifter with 23°/mm phase shift at -2.5V (VpiLpi=1.9V.cm) are achieved while keeping low doping levels in the core of the waveguide to maximize the OMA of the transmitter.

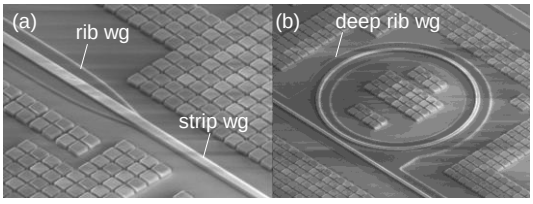

Fig 1 : example of optical structure co-integrated with a self-aligned multi-etching process (a) rib to strip transistion (b) ring resonator using deep rib level

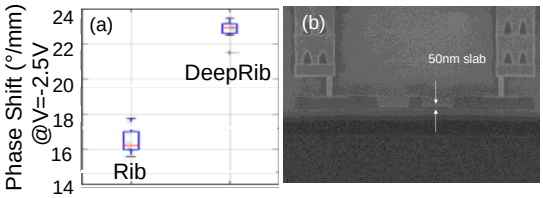

Fig 2 (a) phase shift of rib-wg and deep rib-wg based PN junction phase shifter (b) Deep-rib PN junction phase shifter cross section

3. 193nm Immersion Lithography

The use of advanced lithography in Si-Photonics such as ArF immersion lithography has been proposed in [2]. With such process, one can achieve smaller feature size, for example smaller trenches in Si down to 50nm are shown on fig. 3a. By using apodization technique in designing Single Polarization Grating Couplers (SPGC) [3], this process leads to a 0.2dB insertion loss improvement over a standard SPGC grating coupler. The dispersion of the peak loss was also improved, reducing from a within wafer standard deviation of 0.15dB on reference sample down to 0.05 dB. Together with the use of a proper mask-data-preparation flow, the line edge roughness of waveguides can be also improved. Using this process, the propagation loss of a single mode rib waveguide (W=0.32µm) was reduced

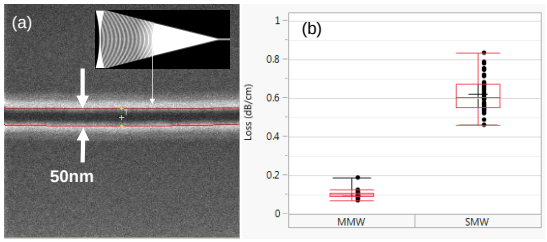

Fig 3 : (a) 50nm trench on SPGC, (b) measured SM rib waveguides and MM rib waveguide loss at λ=1310nm

down to 0.6 dB/cm and 0.1 dB/cm for multi-mode-waveguides (fig. 3b).

4. 3D Si/SiN waveguides

SiN is an attractive material for integrated optics, due to its optical properties: extended transparency range, medium index contrast with SiO2 and low thermal dependency of the optical index. In this work we integrated a 600nm thick SiN layer deposited by PECVD above the Si-level. Two levels of patterning are allowing to define strip, rib waveguides and grating structures [4]. The slab thickness is 320nm (fig. 4). Typical propagation loss in the O-band are 0.6dB/cm for a 0.7µm width 600nm height strip waveguide, and rib waveguide loss are below 0.1dB/cm. Dedicated adiabatic coupler using strip Si and strip SiN waveguides have been designed for optical mode

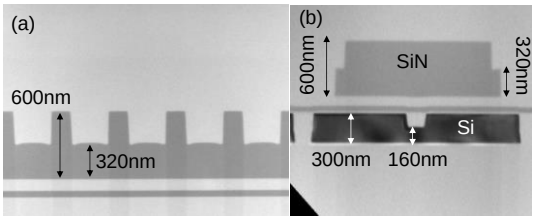

Fig 4 : (a) Dual Etched SiN pattern, (b) Si/SiN pattern with multi-etching

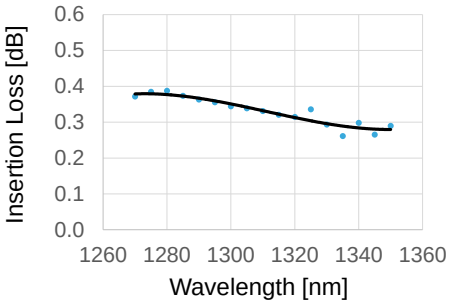

Fig 5 : Si-SiN adiabatic transition loss in the O-Band (TE mode)

transition between the Si and the SiN layers. A maximum transmission loss of 0.4dB for the TE mode in the O-band has been measured (fig 5).

As SiN is featuring a lower refractive index variation with temperature than Si, it can be interesting to

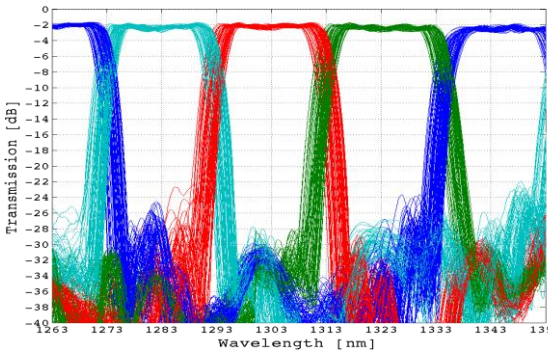

Fig 6: Example of DeMUX using interleaved Mach Zendher structure patterned in the SiN layer

fabricate DeMUX filter for CWDM application using the SiN layer. Fig. 6 is showing an example of integration of DeMUX base on interleaved Mach Zendher interferometer. The device is designed to operate with 4 channels separated by 20nm in the O-Band. Within wafer measurements are showing 2.7dB median insertion loss for a 13nm channel bandwidth and a median 23dB channel isolation. The plateau loss is 2dB.

5. Conclusion

In this work we evaluated the impact of advanced process modules on the device offering of Si-photonics future platform. The use of advanced patterning and the integration of supplementary SiN layer are promising element to improve the performance of Si-Photonics circuits.

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