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Heat Dissipation property of III-V on SiC Platform for Photonic Integrated Circuits

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Abstract

We investigated the heat dissipation properties of III-V on SiC platform. Owing to the high thermal conductivity of SiC, the temperature increase in the InP layer on the SiC wafer was approximately 9 times smaller than that on the SiO_2/Si wafer. The high heat dissipation efficiency of the III-V on SiC platform can significantly improve the thermal properties of III-V photonic integrated circuits.

1. Introduction

InP-based photonic integrated circuits (PICs) are able to monolithically integrate passive waveguide components and active waveguide components such as laser diodes (LDs), modulators, and photodetectors, which is one of the advantages against Si PICs. However, the weak optical confinement of an InP-based waveguide has prevented us from developing ultrasmall PICs. To achieve the strong optical confinement like a Si waveguide on a Si-on-insulator wafer, we have proposed the III-V CMOS photonics platform [1] which uses a III-V on insulator wafer as shown in Fig. 1(a). Since a thin InP-based layer is bonded on an SiO_2/Si wafer, we can achieve the strong optical confinement which enables the miniaturization of InP photonic devices [2, 3]. Active waveguide components such as LDs [4], modulators [5, 6], PDs [7] have been also reported by forming a lateral PIN junction on a III-V-OI wafer. However, one of the obstacles of the III-V CMOS photonics platform is its poor thermal dissipation, which is in particular critical for LDs.

To overcome the poor thermal dissipation in the III-V-OI platform, we have proposed the III-V on SiC platform [8] as shown in Fig. 1(b). The SiO_2 BOX is replaced by a SiC bulk wafer, which works as a waveguide under cladding layer and a heat sink. Since the thermal conductivity of SiC is more than 100 times greater than that of SiO_2, the heat dissipation in the III-V on SiC platform is expected to be significantly improved. In addition, the thermal stress induced by the difference in the thermal expansion coefficient between InP and Si can be reduced by using SiC as a handle wafer. However, the properties of the III-V on SiC platform have yet been examined experimentally yet. In this paper, we fabricate a III-V on SiC wafer by wafer bonding and report its thermal properties to show the feasibility of the III-V on SiC platform

2. Fabrication of III-V on SiC wafer

We first examined the fabrication procedure of III-V on SiC wafer. In this study, we used a semi-insulating 6H SiC wafer to avoid the free-carrier absorption. The root mean square of the surface roughness of a SiC wafer was 0.18 nm, which was small enough for direct wafer bonding. Fig. 2 is the fabrication procedure of a III-V on SiC wafer. We prepared an epitaxial InP wafer containing a thin device layer (in this case, a 220-nm-thick InP layer) and an InGaAs etch stop layer. After cleaning InP and SiC wafers, we deposited a 3-nm-thick Al_2O_3 layer on both wafers as a bonding interface. Then, the prebonding annealing at 600 °C at was carried out for outgassing from the Al_2O_3 layers [9]. After cleaning the surfaces by ultrasonic water, the InP wafer was bonded on the SiC wafer followed by the postbonding annealing at 300 °C. Finally, an InP substrate and an etch stop layer were selectively removed by wet etching. A photo of the III-V on SiC wafer is also shown in Fig. 2.

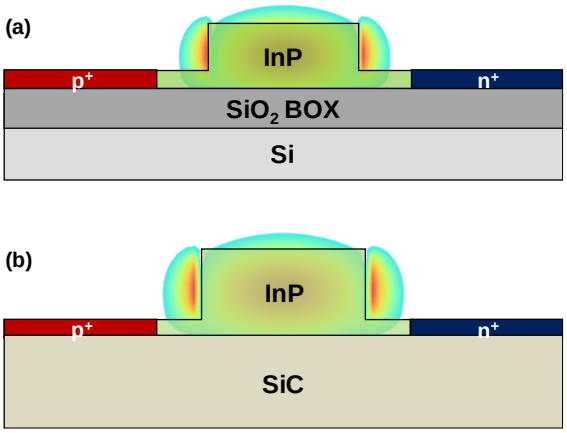

Fig. 1 (a) III-V on SiO_2/Si platform and (b) III-V on SiC platform for photonic integrated circuits.

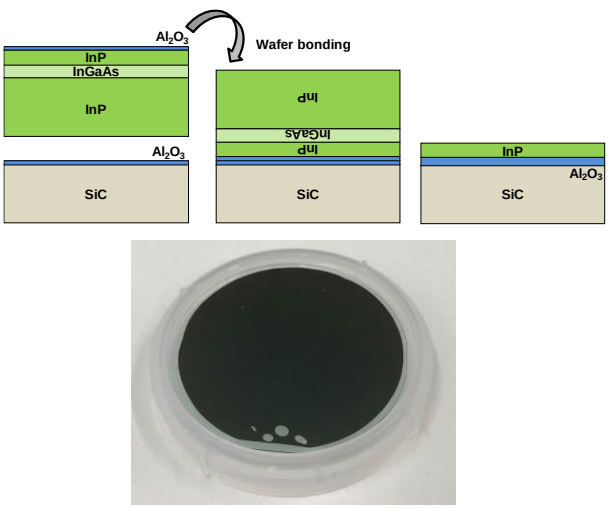

Fig. 2 Fabrication procedure and photo of III-V on SiC wafer.

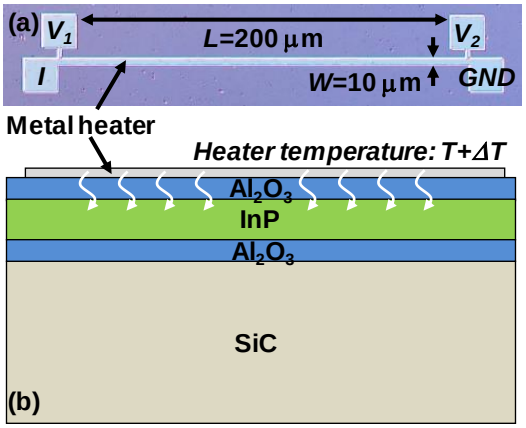

Fig. 3 Plan-view photo and cross-sectional schematic of resistance temperature detector on InP on SiC wafer.

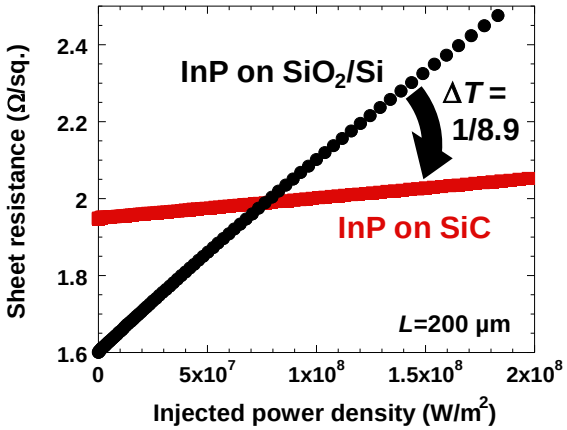

Fig. 4 Measured sheet resistance of resistance temperature detector on InP on SiC and InP on SiC wafers.

3. Evaluation of heat dissipation

To evaluate the heat dissipation of the InP on SiC wafer, we prepared a resistance temperature detector by depositing a metal heater on the top of wafer. An increase in the resistance of a metal heater is proportional to an increase in its temperature. Thus, we can evaluate the heat dissipation property of the InP on SiC. A plan-view photo and cross-sectional schematic of the fabricated test device are shown in Fig. 3. After capping the surface of the wafer by Al_2O_3, a 100-nm-thick Ti/Pt metal layer was deposited on the top by sputtering. Finally, the heater pattern was formed by lift-off. The length and width of the heater were designed to be 200 µm and 10 µm, respectively. We prepared a four-terminal Kelvin test structure to evaluate a resistance of the meatal heater and an injected power into the metal heater accurately [10]. For comparison, we prepared the same metal heater on the InP on SiO_2/Si wafer.

The measured sheet resistance of the metal heater as a function of the injected power density is shown in Fig. 4. As expected, the sheet resistance was proportional to the injected power, enabling the evaluation of the heat dissipation from its slope. As shown in Fig. 4, the heat dissipation of the InP on SiC sample was 8.9 times bettern than that of the InP on SiO_2/Si sample.

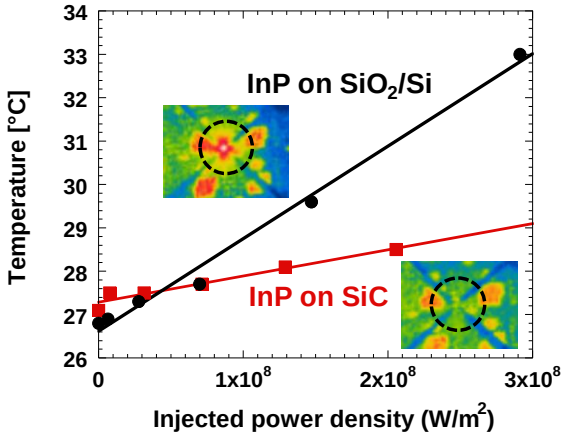

Fig. 5 Device temperature as a function of injected power density measured by thermal camera.

The device temperature was also directly evaluated by observing the sample from the top using a thermal camera. The thermal images are shown in insets of Fig. 5. We observed a hot spot on the InP on SiO_2/Si sample, while there was no obvious hot spot on the InP on SiC sample. From the thermal image, we estimate the device temperature as shown in Fig. 5. Although the difference in temperature between SiO_2/Si and Si was smaller than expected because of the low resolution of the thermal camera, the device temperature of the InP on SiC samples was significantly smaller than that of the InP on SiO_2/Si samples.

4. Conclusions

We have successfully demonstrated the significant improvement in the heat dissipation by replacing a SiO_2/Si wafer by a SiC wafer. Thus, the III-V on SiC platform is promising for high-density photonic integrated circuits.

Acknowledgements

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References

[1] M. Takenaka and Y. Nakano, Opt. Express **15** (2007) 8422.

[2] M. Takenaka, M. Yokoyama, M. Sugiyama, Y. Nakano, and S. Takagi, Appl. Phys. Express **2** (2009) 122201.

[3] M. Takenaka, M. Yokoyama, M. Sugiyama, Y. Nakano, and S. Takagi, Appl. Phys. Express **6** (2013) 42501. [1] S. Matsuo, T. Fujii, K. Hasebe, K. Takeda, T. Sato, and T. Kakitsuka, Opt. Express **22**, 12139 (2014).

[4] S. Matsuo, T. Fujii, K. Hasebe, K. Takeda, T. Sato, and T. Kakitsuka, Opt. Express **22** (2014) 12139.

[5] Y. Ikku, M. Yokoyama, O. Ichikawa, M. Hata, M. Takenaka, and S. Takagi, Opt. Express **20**, B357 (2012).

[6] J.-K. Park, S. Takagi, and M. Takenaka, Opt. Express **26** (2018) 4842.

[7] D. Inoue, T. Hiratani, Y. Atsuji, T. Tomiyasu, T. Amemiya, N. Nishiyama, and S. Arai, IEEE J. Sel. Top. Quantum Electron. **21** (2015) 392.

[8] M. Takenaka and S. Takagi, Opt. Express **25** (2017) 29993.

[9] J. Han, M. Takenaka, and S. Takagi, Jpn. J. Appl. Phys. **55** (2016) 04EC06.

[10] C. S. Tan, Microelectron. Eng. **87** (2010) 682.