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III-V/Si Photonic Integration Platform for On-Si Laser Diodes and High Efficiency Mach-Zehnder Modulators

Tatsurou Hiraki[1, 2], Takuma Aihara[1], Koji Takeda[1, 2], Takuro Fujii[1, 2], Takaaki Kakitsuka[1, 2], Tai Tsuchizawa[1, 2], Hiroshi Fukuda[1, 2], and Shinji Matsuo[1, 2]

[1] NTT Device Technology Labs, NTT Corporation
[2] NTT Nanophotonics Center, NTT Corporation
3-1, Morinosato Wakamiya, Atsugi-shi Kanagawa 243-0198, Japan
Phone: +81-46-240-2681 E-mail: tatsurou.hiraki.gu@hco.ntt.co.jp

Abstract

We report a III-V/Si photonic integration platform for an integrated laser diode (LD) and a high-efficiency Mach-Zehnder modulator (MZM) on a Si platform. The direct wafer bonding method provides the integration of the III-V semiconductors and Si. The integrated III-V films enable efficient light emission for the LD and a large carrier induced refractive index change for the MZM. We demonstrate a 500-μm-long InP-based LD on a Si waveguide, whose output power is over ~4 mW, and a high-efficiency III-V/Si metal-oxide-semiconductor capacitor MZM, whose modulation efficiency (0.09 Vcm) overcomes the theoretical efficiency limit of the conventional Si MOS capacitor MZM.

1. Introduction

With the rapidly increasing internet traffic, large-capacity optical fiber links are necessary for sustainable growth of network traffic. This strongly requires reductions in the cost, size, and power consumption of the optical transceivers, including the laser diodes (LDs) and Mach-Zehnder modulators (MZMs). The Si photonics platform is attractive for reducing the cost and size of the photonic integrated circuits because of its highly confined Si waveguides and mass productivity on large-size silicon-on-insulator (SOI) wafers. However, on the platform, the lack of LDs on Si and poor modulation efficiency of Si MZMs limit to reduce the assembly cost and power consumption of the optical transceivers, respectively. To overcome the issues, heterogeneous integration of InP-based materials on a SOI wafer is strongly required. They have direct bandgap structures and therefore enable efficient light emission. In addition, since their effective masses are smaller than Si's, the carrier induced optical phase shifts are larger than those of Si. In this paper, we review our recent works on III-V/Si LDs and MZMs using the membrane InP-based layer. The membrane layer provides easy integrations of the LDs and MZMs with the Si waveguides, and large optical confinement factor for the efficient interaction between photons and carriers. In following section, we demonstrate a membrane InP-based LD on a Si waveguide, whose thickness is almost consistent with the typical SOI wafer [1]. In addition, we also use a membrane InGaAsP layer to form a metal-oxide-semiconductor (MOS) capacitor MZM, which overcomes the efficiency limit of conventional Si MOS capacitor MZMs [2].

2. Integrated LD on Si platform

For an LD on the Si platform, a critical issue is efficient optical coupling between the III-V and Si layers. Since the effective refractive index of the typically 2~3-μm-thick III-V layer of the LD is much larger than that of the Si waveguide layer, a complex III-V taper structure is required for optical coupling between III-V and Si layers. To overcome the issue, our approach is to integrate the membrane III-V LD, whose III-V semiconductor thickness is almost comparable to that of the Si waveguide layer. Figure 1 shows a schematic of the membrane InP-based LD, optically coupled to the Si waveguide [1]. The 0.23-μm-thick InP film is located above the 0.2-μm-thick Si waveguide, and the multiple-quantum well (MQW) layer is buried in the InP layer. Since the effective refractive indices of the two semiconductor layers are almost matched, the light emitted from the LD is easily coupled to the Si waveguide by using a reasonably thin InP taper geometry, whose tip width and length are ~100 nm and 200 μm, respectively. The lateral current-injection p-i-n diode is designed to avoid the optical absorption of the metal electrodes on the membrane InP layer. The LD has a silicon nitride (SiN) grating region to construct a distributed feedback (DFB) LD.

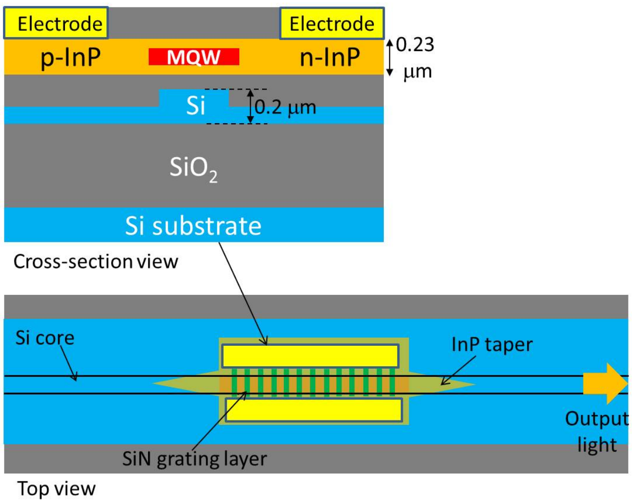

Fig. 1. Schematic of membrane LD on Si [1].

The fabrication process is as follows. First, the Si waveguide layer is patterned on the SOI wafer. Then, the cladding film is deposited, followed by chemical mechanical polishing. Next, the MQW layer on the InP wafer is bonded to the SOI wafer by using the oxygen-plasma-assisted bonding method. After that, the MQW layer is patterned then buried by regrowth of an InP layer. Next, the donor and acceptor regions are formed in the InP layer by using Si ion implantation and Zn diffusion, respectively. Then, a hydrogen free SiN film is deposited [3], followed by the patterning for the grating. Finally, the electrodes and overcladding film are formed. Fig. 2 shows a cross section scanning electron microscope (SEM) image of the fabricated laser diode [1].

We measured the output power of a fabricated DFB LD with an active layer length of 500 μm. In the measurement, we used a lensed fiber to couple to the output light. The fabricated device showed the fiber output power of over 4 mW at room temperature. Notably, thanks to the small active volume, the small threshold current contributes to suppress the increase of active-region temperature in the membrane layer and lasing up to 130 degrees Celsius [1].

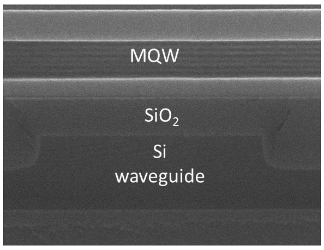

Fig. 2. Cross-sectional SEM image of fabricated LD [1].

3. High-efficiency MZM on Si platform

For a high-efficiency MZM on the Si platform, it is important to enhance the carrier-induced refractive index change without increasing the optical loss. We focused on the InGaAsP layer, whose electron effective mass is smaller than that of Si. This is beneficial for increasing the carrier plasma effect and thus enhancing the carrier induced refractive index change. In addition, the InGaAsP film has a large band-filling effect, which also causes the refractive index change. These two effects enable us to reduce the $V_\pi L$ of the MZM. Notably, the high electron mobility of the InGaAsP film contributes to reducing the free carrier absorption loss. This means the modulation efficiency is improved without increasing the optical loss. We used the n-type InGaAsP film, whose photoluminescence peak was around 1.3 μm, for the MOS capacitor MZM on the Si platform. Figure 3(a) shows a cross-section view of the proposed InGaAsP/Si MOS capacitor MZM [2]. The n-type InGaAsP layer is bonded to the 10-nm-thick SiO_2 insulator on the p-type Si. This structure can be fabricated by the wafer bonding method. The two semiconductor layers were patterned to form a waveguide region with a single-mode condition. The calculated mode field pattern is shown in Fig. 3(b). In this device, the accumulated majority carriers at the semiconductor/SiO_2 interfaces shift the phase of the propagated light. To maximize the overlap between the optical intensity and carrier distribution, the thicknesses of the two semiconductors are set for effective refractive index matching and high optical confinement. Here, the InGaAsP and Si layer thicknesses are 100 and 110 nm, respectively. The MOS capacitor phase shifters are integrated with the Si waveguide multi-mode interferences (MMIs), as shown in Fig. 3(c). The InGaAsP tapers are used for coupling between them. Thanks to the effective index matching between the two semiconductor layers, they are easily optically coupled with the reasonably narrow InGaAsP taper, whose tip width and length are ~100 nm and 80 μm, respectively.

We measured $V_\pi L$ of the fabricated MZM. The measured $V_\pi L$ is 0.09 Vcm, which is over three times smaller than that of the conventional Si MOS capacitor MZM. The insertion loss of the MZM, whose phase shifter length is 700 μm, is around 2 dB. The loss is also lower than that of the conventional Si MZM. These results show that using the InGaAsP layer improves the modulation efficiency without increasing the insertion loss [2].

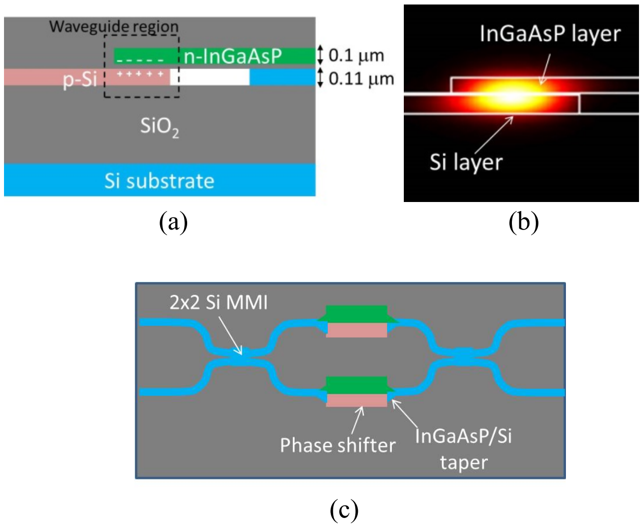

Fig. 3. (a) Cross-section view, (b) calculated mode field pattern, and (c) top view of InGaAsP/Si MOS capacitor MZM [2].

4. Conclusions

We reviewed our InP-based LD integrated on a Si waveguide and our high-efficiency III-V/Si MOS capacitor MZM. The approach is promising for constructing low-cost and low-power optical transceivers on the Si platform.

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Reference

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