Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp549-550

Investigation of Delay Issue in Pure-CMOS One-Time Configuration FPGA with Large Crossbar Switch Array

Ying-Hao Ho, Masato Oda, Shinichi Yasuda

Toshiba Corporation,
Frontier Research Laboratory, Corporate R&D Center, R&D Division,
1, Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 212-8582, Japan
E-mail:yinghao.ho@toshiba.co.jp

Abstract

A study of the delay issue that accompanies increasing array size in transistor-based antifuse one-time configuration (OTC) crossbar FPGA is presented. The principle reason for delay is identified as the rectification properties of antifuse CMOS (OTC memory) by confirming the bidirectional resistance of every programmed cell. Processing speed is improved by more than 10^3x and a benchmark circuit (filter) is successfully demonstrated on OTC-FPGA by eliminating the rectification properties of antifuse transistor cell.

1. Introduction

Field programmable gate arrays (FPGA) have attracted much attention because of their high performance in parallel calculation and their wide variety of applications such as edge computing [1][2]. Crossbar architecture FPGA based on transistor-based antifuse could be the best solution owing to its advantages in terms of low power consumption, high circuit density [3], and suitability for pure-CMOS process. Thanks to the high-temperature/-noise resistance, OTC-FPGA, even only one-time programmable, is highly anticipated to be used in special environment. In order to improve the routability of OTC-FPGA, a larger crossbar array is strongly desired. However, instead of hard breakdown (HBD), soft breakdown (SBD) of MOS transistor is prone to occur as the influence of the peripheral circuit becomes significant [4]. In this study, a transistor-based antifuse crossbar array with 224 inputs, which is over 3x larger than the one in the previous study [3], has been investigated. The delay issue that accompanies increasing array size has been confirmed and the rectifying properties of OTC memory has been identified as one of the major issues in OTC-FPGA performance. By reprogramming the specific OTC memory, the delay in benchmark circuit is reduced 10^3x.

2. OTC-FPGA technology

The circuit of the antifuse-based crossbar array in the proposed OTC-FPGA is shown in Fig. 1a. The OTC memory, located at the intersection of row line and column line, is composed of standard-voltage nMOS transistors. To avoid unexpected breakdown, high-voltage transistors are used for applying program voltage (Vprg); in order to improve the circuit density, other areas of the crossbar array consist of standard transistors. Additionally, as connecting of only one input is allowed in each output line of an FPGA crossbar array, local selector is not required, and it is beneficial in terms of reducing the array size considerably. The layout of the crossbar area is shown in Fig. 1b.

The micrograph of the chip fabricated by pure-CMOS process in 130nm node is shown in Fig. 2a. Fig. 2b depicts the basic block architecture of the test chip; one basic block includes 10 4-input LUTs and 20 flip-flops. Local switch blocks (LSBs) and global switch blocks (GSBs), which consist of OTC crossbar array, are deployed in the basic block. LSBs connect GSBs and logic elements in the same basic block; GSBs transmit data between basic blocks. In this study, GSBs with 224 inputs, more than 3x larger than the one in the previous report, are designed.

3. Experiment and Discussion

In order to implement the test logic to OTC-FPGA, arbitrary logic, designed in Verilog HDL code, is configured by the implementation flow shown in Fig. 3. The measured waveform of 2-bit adder implemented on OTC-FPGA is shown in Fig. 4. The delay in the rising edge (△d1) in OUT0 is around 3ms, while the delay in falling edge (△d2) is not observable in the same scale. The inconsistency between the delays of two edges implies that some OTC memory cells with rectification properties locate in the path of data transmission in the SBs.

In order to clarify this issue, it is important to define the range in which the OTC memory operates with rectification properties. Bidirectional resistance of the OTC memory unit has been measured by the structure shown in Fig 5(a). Resistance after breakdown of the OTC memory was controlled by connecting external resistance to the gate terminal of memory cell. Fig. 5(b) indicates that the resistance from source/drain to gate, defined as reverse resistance, will be 10x to 10^4x larger than the resistance from gate to source/drain, defined as forward resistance, in case the forward resistance becomes larger than 300kΩ.

Although only the forward resistance is measurable in crossbar array as shown in Fig. 1a, reducing the rectification properties is possible. Fig. 6 shows that by reprogramming the OTC memory cell with longer data pulse, the reverse resistance becomes closer to forward resistance.

Finally, the improvement strategy was executed on OTC-FPGA. The forward resistance of all the programmed OTC memory cells located in the path of data transmission has been confirmed. As indicated in Fig. 7, the resistance of the OTC memory increases with the increase of the distance from the selected OTC memory to the high-voltage pMOS. By reprogramming the memory cell with the resistance higher than 300kΩ, the resistance of memory cells is reduced around 67%-91%, while the delay of 2-bit adder decreases over 10^4x, from 3ms to 90ns, as Fig. 4c indicates.

Fig. 8 shows that benchmark circuit (filter) has been implemented successfully on OTC-FPGA and the delay has been reduced more than 10^3x after eliminating rectification properties.

4. Conclusions

We have investigated the delay issue that accompanies the increasing array size of OTC-FPGA. Large-scale crossbar switches are prone to rectifying properties. By eliminating the rectification properties of transistor-based antifuses located in SBs, the operation speed has been improved 10^3x.

References

[1] X. Bai et al., Symposium on VLSI Technology, pp.T28-T29, 2017

[2] A. Ledeczi et al., IEEE Sensors Journal, No.9 p.1370, 2009.

[3] S. Yasuda et al., IEEE Symposium on VLSI Technology, pp.24-25, 2016.

[4] A.Toriumi et al., Science and Technology of Advanced Materials, pp.181-186, 2000.

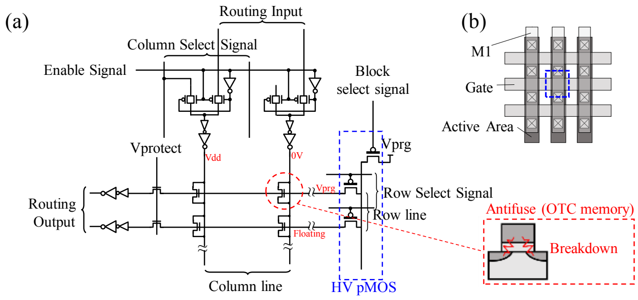

Fig. 1. (a) Elementary diagram of transistor-based antifuse crossbar array. (b) Layout of crossbar antifuse array.

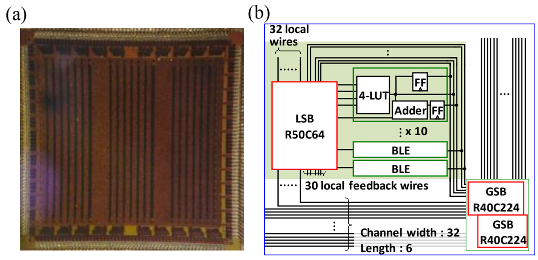

Fig. 2. (a) Chip micrograph of OTC-FPGA test circuit fabricated in 130nm CMOS process. (b) Basic block architecture of the test chip.

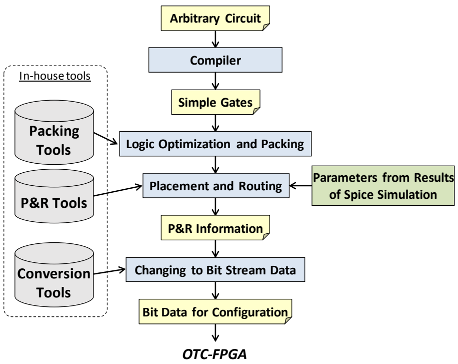

Fig. 3. Implementation flow of OTC-FPGA. In-house CAD tool including P&R tools applicable for the OTC crossbar FPGA architecture was developed.

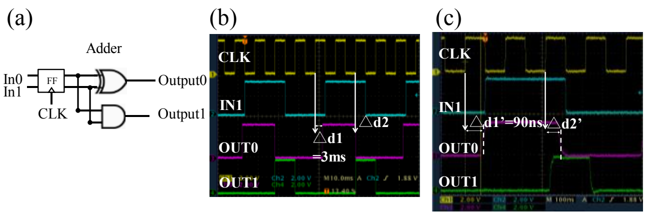

Fig. 4. (a) The predetermined circuit implemented on OTC-FPGA. (b) The measured waveform before and (c) after implementation improvement strategy.

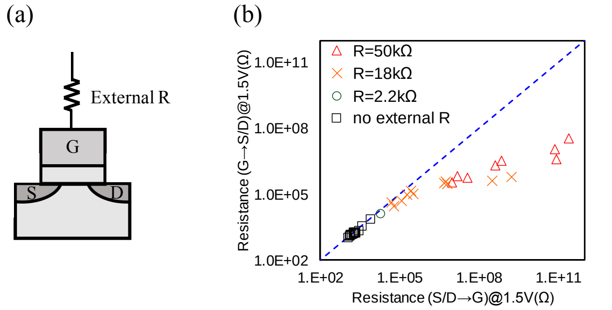

Fig. 5. The relationship between forward resistance and reverse resistance of OTC memory. The rectification property becomes significant when forward resistance is over 300kΩ.

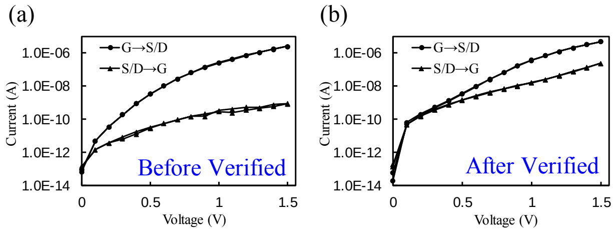

Fig. 6. The I-V characteristic of OTC memory before (a) and after (b) verification. The rectification property is reduced by applying longer programming signal.

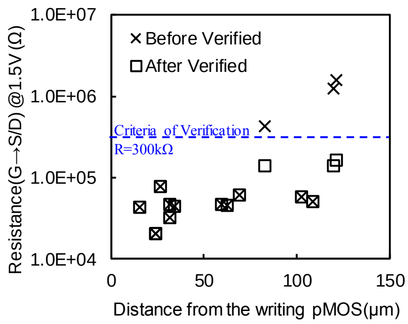

Fig. 7. The dependence between resistance of OTC memory in the SBs on adder circuit and the distance from the HV pMOS. The memory cell with resistance higher than 300kΩ is verified by applying longer writing signal.

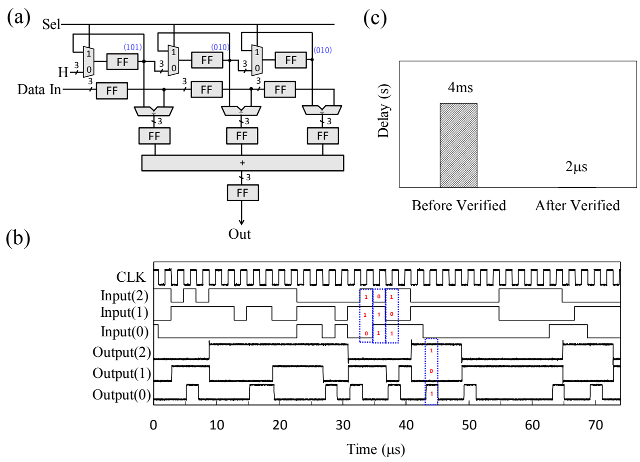

Fig. 8. (a) The benchmark circuit (filter) circuit implemented on OTC-FPGA. (b) The measured waveform of filter operation after executing improvement strategy. (c) The comparison of delay before and after executing improvement strategy.