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Carbon nanotube based high performance CMOS and optoelectronic devices and integrated systems

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Abstract

High purity semiconducting single walled carbon nanotubes (s-SWCNTs) have been used as active channel materials for various electronic and optoelectronic devices, including field-effect transistors (FETs), light emitting diodes and photodiodes, and as a general platform for building three-dimensional optoelectronic integrated system.

1. Introduction

Carbon nanotube (CNT)-based electronics has been considered one of the most promising candidates to replace Si complementary metal-oxide-semiconductor (CMOS) technology, which will soon meet its performance limit. In addition, CNTs are direct band gap materials making them promising to make significant impact on the developments of nanoscale optoelectronic devices. In particular CNTs have been investigated for various electronic and optoelectronic device applications, such as sub-10nm CMOS devices which outperform that of state-of-the-art Si based CMOS devices in both speed and power consumption [1-5], as well as idea material for monolithic optoelectronic integration with complementary MOS-compatible signal processing circuit [6-8].

2. High speed and low-power electronic devices

Prototype device studies on individual CNTs revealed that CNT based devices have the potential to outperform Si CMOS technology in both performance and power consumption. With a well-designed device structure and in combination with graphene, we showed that high-performance top-gated CNT FETs with a gate length of 5 nm can be fabricated. A scaling trend study revealed that sub-10 nm CNT CMOS FETs significantly outperform Si CMOS FETs (Figure 1 and Figure 2). In particular, the 5 nm CNT FETs approach the quantum limit of FETs and involve only approximately one electron per switch. The contact length of the CNT CMOS devices has been scaled down to 25 nm, and the smallest CMOS inverter yet reported with a total pitch size of 240 nm is demonstrated. These results show that CNT CMOS technology has the potential to substantially outperform that of Si when approaching the quantum limits of a binary logic switch and to extend mainstream CMOS technology in the post-Moore era [1].

Significant progress has also been made in fabricating carbon nanotube low-power devices. An efficient way to reduce the power is to lower the supply voltage V_{DD}, but this voltage is restricted by the 60 millivolts per decade thermionic limit of subthreshold swing (SS) in FETs. A Dirac source (DS) with a much narrower electron density distribution around the Fermi level than that of conventional FETs was recently proposed and demonstrated using CNT to reduce SS [2]. In particular, a DS-FET with a carbon nanotube channel provided an average SS of 40 millivolt per decade over four decades of current at room temperature and high device current. When compared with state-of-the-art Si 14-nanometer node FETs (Figure 3), a similar I_{on} is realized but at much lower supply voltage of 0.5 versus 0.7 volts for Si, and a much steeper SS below 35 millivolts per decade in the off-state.

3. Optoelectronic devices and integrated electronic and optoelectronic systems

Semiconducting single-wall CNTs are direct band-gap materials, and thus can efficiently absorb and emit light. In addition, extremely efficient carrier multiplication (CM) effect has been observed, which may potentially lead to a higher energy conversion efficiency than that defined by the Shockley-Quiesser limit. More recently, efficient photovoltage multiplication was realized via introducing virtual contacts in CNTs, making the output photovoltage of CNT based solar cells a tunable quantity via choosing the diameter of the tube and the number of virtual contacts introduced in the device [6]. This technique has been utilized to build high performance infrared photodetectors and sensors for shortwave infrared.

An electrically driven carbon nanotube-based on-chip three-dimensional optoelectronic integrated circuit as well as electrically-driven monolithic plasmonic interconnect circuits have been constructed [7-8]. It was demonstrate (Figure 4) that photovoltaic receivers, electrically driven transmitters and on-chip electronic circuits can all be fabricated using carbon nanotubes via a complementary metal oxide semiconductor-compatible low-temperature process, providing a seamless integration platform for realizing monolithic three-dimensional optoelectronic integrated circuits with diversified functionality such as the heterogeneous AND gates. These circuits can be vertically scaled down to sub-30 nm and operates in photovoltaic mode at room temperature. Parallel optical communication between functional layers, for example, bottom-layer digital circuits and top-layer memory, has been demonstrated by mapping data using transmitter/receiver array, which could be extended as the next generation energy-efficient signal processing paradigm.

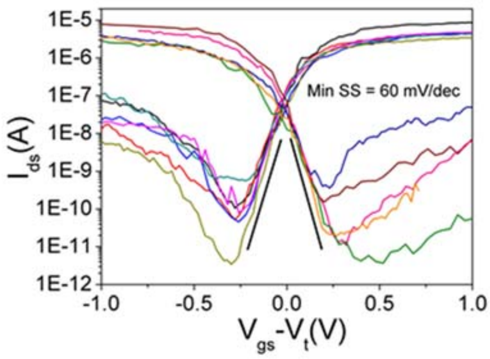

Fig. 1 Transfer characteristics of CNT CMOS FETs at V_{ds} =±0.1 V, these FETs including six n-type FETs and five p-type FETs with gate lengths ranging from 10 nm to 20 nm.

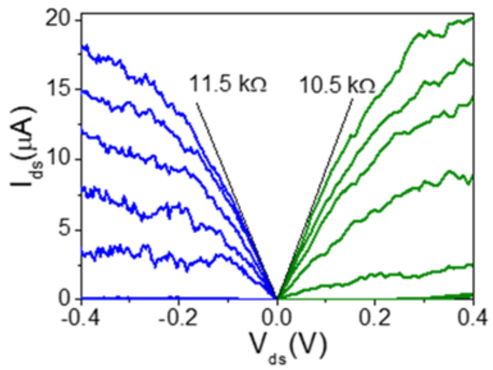

Fig. 2 Output characteristics of a typical pair of 10 nm n-type and p-type CNT CMOS FETs.

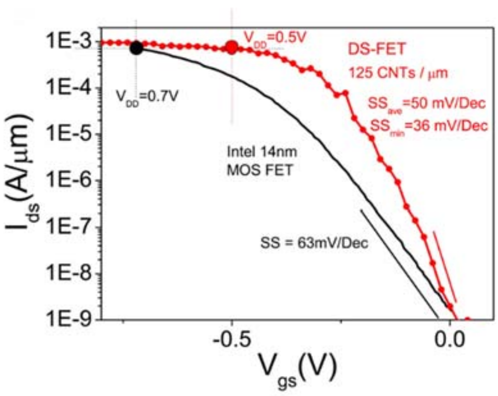

Fig. 3 Comparison between a 400 nm DS-FET and commercial Intel 14 nm Si MOS FET. Si MOS FET (black) was powered by 0.7 V, while DS-FET (red) was powered by a low bias of 0.5 V.

4. Conclusions

To summarize, using semiconducting CNTs and a well developed CMOS-compatible doping-free fabrication technique, we have realized high performance and low-power electronic devices, which outperform state-of-the-art Si based electronic CMOS devices; photovoltaic receivers, electrically driven transmitters, and demonstrated monolithic 3D optoelectronic integrated circuits..

Acknowledgements

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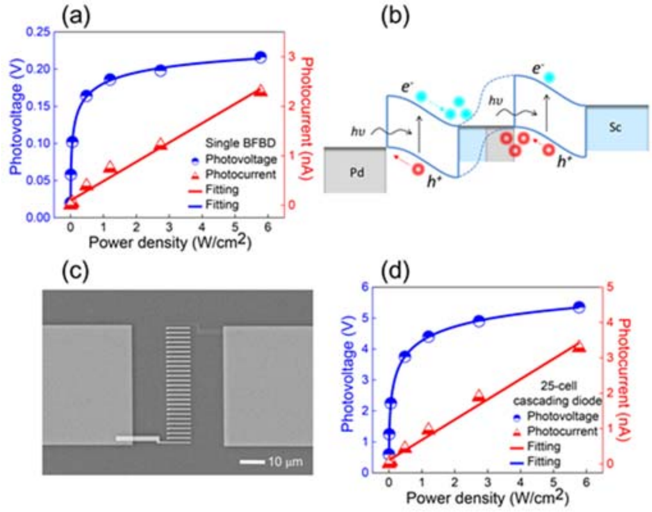

Fig. 4 (a) Experimental and fitted results of photocurrent and photovoltage as a function of IR power density with λ = 1800 nm for a single CNT thin film diode. (b) Energy band diagram illustrating the role played by the virtual contact under incident illumination. (c) SEM image of a 25-cell cascading diode. (d) Experimental and fitted results of photocurrent and photovoltage versus IR power density for 25-cell cascading diode.

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