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Extremely low power LSI using crystalline oxide semiconductor transistor

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Abstract

A 60-nm-node crystaline-oxide-semicondoctor FET exhibits an extremely low off-state current of 7.0×10^{-23} A/FET at 85°C. A memory device made with the 60-nm-node OSFET and a 3.5 fF cell capacitor retains data for more than 1 h at 85°C, rewrites data at under 5 ns, writes data with energy as low as 2.5 fJ per cell, and endures more than 10^{14} writes. A low-power chip prototyped with a hybrid process of 65 nm CMOS process and 60 nm crystaline-oxide-semicondoctor process can reduce its standby power to the order of nanowatts through power gating. Crystaline-oxide-semicondoctor technology can be used to construct NMOS-only functional circuits in the BEOL process, and is expected to enable a wide range of applications. It is a promising candidate as a technology that can reduce power consumption of the hardware to meet the demands of AI and IoT applications.

1. Introduction

The recent boom in AI and IoT increases the amount of data to be processed, and ICs that can process deep-learning operations fast and with low power are much sought after.

To meet the demand for low-power ICs, we turned our attention to crystalline-oxide-semiconductor FETs (OSFETs), which have extremely low off-state current. The OSFET is already being widely mass produced in the display field. To extend the OSFET's application range into the IC field, however, the OSFET needs to be scaled down to technology nodes beyond 100 nm. This paper will report the performance and IC application of an L = 60 nm OSFET.

2. Off-state current of the OSFET

The channel region of the OSFET described in this paper specifically is *c*-axis aligned crystalline In-Ga-Zn oxide(CAAC-IGZO). This OSFET has an extremely low off-state current (I_{OFF}), and previous work has discussed its scaling down to L = 30 nm[1]. Fig. 1 plots the temperature dependence of the I_d-V_g curve of an L/W = 60 nm/60 nm OSFET. Unlike the SiFET, the on-state current (I_{ON}) increases at high temperature in the OSFET. Furthermore, even at a high temperature of 192°C, the I_{OFF} is below the lower detection limit of the measurement equipment. To measure the I_{OFF} at such a low level, we have fabricated a test device that allows voltage monitoring of a storage capacitor with a source follower circuit[2]. From the measurement results, the leakage current of one W/L = 60 nm/60 nm OSFET was calculated to be 7.0×10^{-23} A at 85°C (Fig. 2). This value is lower than the I_{OFF} of a common SiFET by more than 10 digits.

3. Application to memory devices

The extremely low I_{OFF} of the OSFET enables a memory device that stores a voltage level stored in a capacitor.

Figure 3 shows a circuit diagram of a 1-bit memory-cell test device and its endurance[3]. The results indicate that even after 10^{14} rewrites of SN voltage, the voltage range of data "0" and "1" did not change. The endurance of 10^{14} times makes the OSFET applicable to almost all applications.

The threshold voltage of the cell transistor can be adjusted with a back gate (Fig. 4). Applying a negative voltage to the back gate allows data retention for a long time even when the front gate is at 0 V. Operating the circuit at normally-off (Noff) mode, where the peripheral circuits are powered down during standby[4], can reduce the standby power of the circuit.

For reliability, the OSFET has exhibited a V_{sh} (V_g value when $I_d = 10^{-12}$ A and V_d = 1.2 V) variance of under 100 mV in a +GBT stress test at 2.75 V, 150°C and for 200 hours (Fig. 5).

4. Chip prototype

We have prototyped a chip that includes an ARM Cortex-M0 core with state-retention flip-flops (FF) and 8 KB embedded memory using OSFET (Fig. 6) [5, 6]. We used a hybrid process with UMC 65 nm Si and SEL 60 nm OS process technologies. OSFETs were fabricated in the BEOL layers (Fig. 7).

The embedded memory was a DRAM-like 1T1C memory cell, which we term DOSRAM. The cell array of DOSRAM does not include Si transistors and thus can be stacked over Si circuitry. The prototype chip had DOSRAM cell array stacked over Si sense amplifier array, allowing the arrays to be divided without area overhead, reducing the bit-line capacitance. The prototype chip's DOSRAM operated with a cycle operating frequency of 100 MHz when the cell capacitance was 3.5 fF[6].

A DRAM cell loses its data through cell leakage. This necessitates refresh operations, where data are written back to the cells with an interval of around 64 ms (embedded applications tend to have higher refresh rates). The

DOSRAM in the prototype had an error bit rate lower than 0.05% after 1 h retention at V_g = 0 V and 85°C[5]. DOSRAM enables sparser refresh than DRAM, rendering power and performance overheads induced by refresh operations practically negligible.

Energy needed for the data rewrite would be the energy needed to charge and discharge the cell capacitor. When V_{DD} = 1.2 V, the rewrite energy per cell would be calculated as 2.5 fJ.

Table 1 compares DOSRAM to other emerging memory devices[7]. DOSRAM is particularly advantageous in endurance and write energy. The retention time of 1 h at 85°C would be effective for reducing the power consumption through Noff operation.

We can enable FF circuits in the CPU core to operate in Noff mode without area overhead by simply adding backup circuits with OSFETs and capacitors. At a chip level, when the active time to sleep time ratio is assumed as 1:1000, the chip operating in Noff mode can reduce power by 94% from when the chip is driven with clock gating, as shown in Fig. 8. This makes the Noff mode particularly effective in applications that drive the chip intermittently, such as IoT.

Table 2 compares this work to similar reports[8, 9].

5. Conclusions

OSFET enables a low-power memory device with unlimited endurance. In addition, the OSFET has high on/off ratio and low Ioff even at high temperatures, and allows construction of functional circuitry in BEOL layers in Si process, or with OSFETs only. Therefore, OS technology is a promising technology with various application possibilities in this market environment that has AI and IoT demanding low power, extending beyond memory applications to applications not possible with SiFETs.

References

[1] D. Matsubayashi *et al.*, *IEDM Dig. Tech. Papers* (2015) 141.
[2] K. Kato *et al.*, *Jpn. J. Appl. Phys.* **51** (2015) 021201.
[3] S. Maeda *et al.*, *ISSCC Dig. Tech. Papers* (2018) 484.
[4] H. Tamura *et al.*, *IEEE Micro*, vol. 34, (2014) 42.
[5] T. Onuki *et al.*, *VLSI Dig. Tech. Papers* (2016) C124.
[6] S. H. Wu *et al.*, *VLSI Dig. Tech. Papers* (2017) T166.
[7] M.-F. Chang, *ISSCC Tutorial T2* (2018).
[8] N. Sakimura *et al.*, *ISSCC Dig. Tech. Papers* (2014) 184.
[9] Y. Liu *et al.*, *ISSCC Dig. Tech. Papers* (2016) 84.

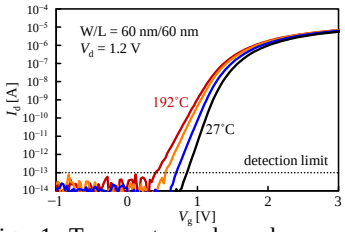

Fig. 1 Temperature dependence of OSFET's I_d-V_g curves

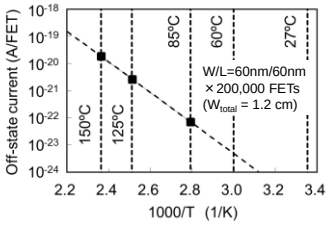

Fig. 2 Arrhenius plot of OSFET's I_{off}

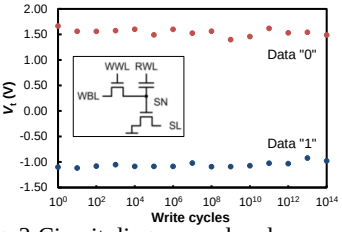

Fig. 3 Circuit diagram and endurance test result of 1-bit memory-cell test device

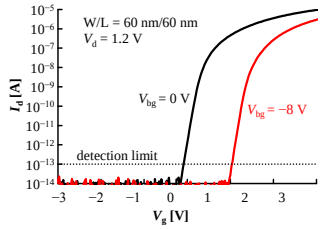

Fig. 4 V_{bg} dependence of OSFET's Id-Vg curves

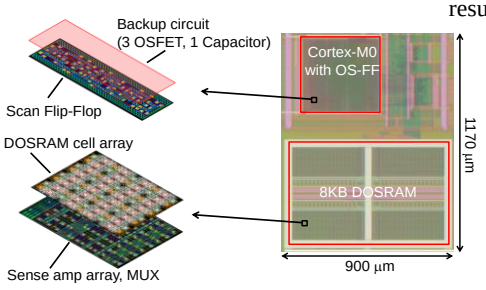

Fig. 6 Die photo of NoffCPU + DOSRAM and layout of area with Si-OS circuit stack

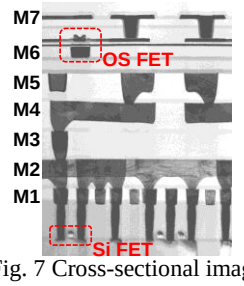

Fig. 7 Cross-sectional image of prototype chip

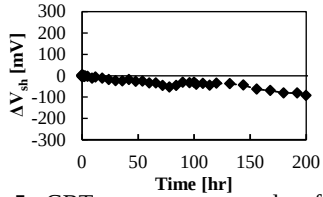

Fig. 5 +GBT measurement results of OSFET

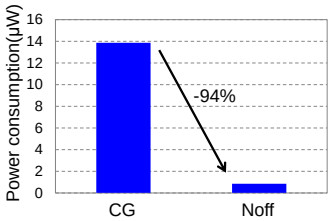

Fig. 8 Power consumption of prototype chip. Active/standby ratio = 1/1000, comparison of clock gating to power gating

Table 1 Comparison between OS memory and other emerging memories

	DOSRAM	MRAM [7]	ReRAM [7]	PCM [7]
Endurance	**> 10^{14}**	**10^{8} to 10^{15}**	**10^{2} to 10^{12}**	**10^{3} to 10^{10}**
Write energy	**2.5 fJ/bit ***	**> 100 fJ**	**> 100 fJ**	**> 10 pJ**
Write time	**< 5 ns ***	**2 ns to 200 ns**	**5 ns to 2 us**	**100 ns to 10 us**
Data retention	**> 1 h@85℃**	**Years**	**Months to Years**	**Years**

* Cell capacitance = 3.5 fF

Table 2 Comparison to similar reports

	[5, 6]	[8]	[9]
Memory device	DOSRAM	MRAM	ReRAM
Technology (Si)	65 nm	90nm	65 nm
Core architecture	Cortex-M0 with OS-FF	16b RISC with nv-FF	8051 with nv-FF
Memory capacity	8 KB	64 KB	8 KB
Clock frequency (MHz)	30-100	20	100
Active power (µW/MHz)	28.2-41.6	145	33
Standby power (µW)	0.02-0.009	1.6	N/A