

High mobility ($>30 \text{ cm}^2/\text{Vs}$) and Low S/D Parasitic Resistance In-Zn-O BEOL Transistor with Ultralow ($<10^{-20} \text{ A}/\mu\text{m}$) Off Leakage Current

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Abstract

We have demonstrated and experimentally verified the advantages of In-Zn-O (InZnO) channel compared with In-Ga-Zn-O (InGaZnO) for high performance oxide semiconductor (OS) BEOL transistors. High mobility ($>30 \text{ cm}^2/\text{Vs}$) and low source/drain (S/D) parasitic resistance (R_{para}) were achieved by using InZnO channel. Analysis of a Schottky barrier height (SBH) at S/D contact and a band offset at OS/SiO₂ interface suggested that the decreases of R_{para} and on-state gate leakage current may result from the lowering of conduction band minimum by InZnO channel. Moreover, ultralow ($<10^{-20} \text{ A}/\mu\text{m}$) off leakage current characteristics including not only S/D leakage but also gate leakage were confirmed to maintain even though smaller bandgap energy (2.7 eV) of InZnO and thin equivalent oxide thickness (EOT) scaling down to 6.2 nm.

(Keywords: oxide semiconductor, InZnO, InGaZnO)

Introduction

Recently, a wide-bandgap OS has attracted attention as a BEOL transistor (Tr.) because of its unique characteristics i.e., low-temperature process ($<400^\circ\text{C}$) and ultralow off-state current (I_{off}) ($<10^{-22} \text{ A}/\mu\text{m}$) [1-3]. However, electron mobility of the most famous OS InGaZnO is around $10 \text{ cm}^2/\text{Vs}$ and low on-current (I_{on}) limits the applications of OS BEOL Tr.

Figure 1 shows our concept of high-performance OS BEOL Tr. with high I_{on} and ultralow I_{off} . In order to improve I_{on} , not only high-mobility OS channel but also low R_{para} and thin EOT are necessary. Although there are some reports on high mobility OS channels [4, 5], R_{para} have not been investigated. Moreover, impacts of thin EOT ($\sim\text{nm}$) on ultralow I_{off} characteristics of OS Tr. has not been investigated [3]. In this paper, we have demonstrated and experimentally verified the advantages of InZnO channel compared with InGaZnO.

Experiments, Results and Discussion

A. Mobility improvement and Low S/D parasitic resistance

Figure 2 (a) and (b) show a device fabrication process and a TEM image, respectively. Figure 3(a) shows a comparison of mobility between fabricated InZnO Tr. and InGaZnO Tr. with EOT of 39 nm. Mobility of InZnO Tr. showed $33 \text{ cm}^2/\text{Vs}$ at the surface carrier concentration (N_s) of 10^{13} cm^{-2} , which was 2 times higher than that of InGaZnO Tr. Although mobility of InGaZnO Tr. tends to increase as In composition ratio increases as shown in Fig. 3(b), InZnO Tr. achieved higher mobility than InGaZnO Tr. at the same In ratio of 0.56, which suggests that Ga cations may suppress carrier transport via In cations. R_{para} was estimated from the vertical intersection point in $R_{\text{on}}-L_g$ plot as shown in Fig. 4(a). R_{para} decreased as the gate voltage increased. As illustrated in Fig. 4(b), since the potential of OS at S/D contact is modulated by the gate voltage and Schottky barrier becomes narrow as the gate voltage increases, tunneling electron injection increases in addition to thermionic electron injection [6]. Figure 5 shows a comparison of gate voltage dependence of R_{para} between InZnO Tr. and InGaZnO Tr. R_{para} of InZnO Tr. was found to be low. To investigate the origin of R_{para} improvement in InZnO Tr., SBH was extracted by fitting R_{para} behavior at low gate overdrive ($V_g - V_{\text{th}} < 1 \text{ V}$) with the thermionic electron injection model as shown in Fig. 6 [6]. Here we adopted a gate voltage modulation factor as α in the model and used ~ 0.1 as α and $41 \text{ A}/\text{cm}^2\text{K}^2$ as Richardson constant [7]. SBH of InZnO Tr. was estimated to be 0.37 eV, while that of InGaZnO Tr. was 0.49 eV. Figure 7 shows a calculated I_{on} improvement with L_g scaling. InZnO Tr. showed a lower R_{para} as well as higher mobility and is expected to show higher I_{on} by proper L_g scaling.

B. Characteristics of thin EOT devices

Figure 8(a) shows a TEM image of fabricated InZnO Tr. with thin EOT. EOT was estimated to be 6.2 nm from C-V characteristics as shown in Fig. (b). Figure 8(c) shows typical I_d-V_g characteristics of InZnO Tr. with EOT of 6.2 nm. Figure 9(a) shows a comparison of I_g-V_g characteristics between InZnO Tr. and InGaZnO Tr. Compared with InGaZnO Tr., I_g-V_g curve of InZnO Tr. shifted positively by 0.2 V and the gate leakage current was suppressed. Figure 9(b) shows Fowler-Nordheim plot of obtained data in Fig 9(a). Assuming that effective mass m^* is 0.34 [8] both for InZnO and InGaZnO, band offsets were estimated to be 1.58 eV and 1.45 eV for InZnO/SiO₂ and InGaZnO/SiO₂ interface, respectively, which suggested that the suppression of gate leakage current suppression at on-state originated from increased band offset by 130 meV. This value agrees with the difference of SBH of InZnO and InGaZnO estimated in Fig. 6. Figure 10 shows a comparison of band diagram of InGaZnO and InZnO. Here bandgap energy was estimated by REELS analysis. Conduction band minimum (E_c) of InZnO is lower than that of InGaZnO by about 130 meV, which may result in the advantages of low R_{para} and suppression of gate leakage current at on-state.

C. Evaluation of ultralow off-state current characteristics

In addition to thin EOT, since the bandgap energy of InZnO is smaller than that of InGaZnO as shown in Fig. 10, there is concern about a degradation of ultralow off-state current characteristics. As shown in Fig. 11(a), we evaluated ultralow leakage characteristics below detection limits of I_d-V_g measurement by monitoring the floating node voltage (V_{FN}) at different cut-off gate voltage. For voltages ($V_g = 0 \sim -0.4 \text{ V}$) with insufficient cutoff as shown in Fig 11(b), subthreshold leakage current was observed, while gate leakage current occurred for large negative voltages ($V_g < -2 \text{ V}$) as shown in Fig. 11(c). Figure 12 shows I_d-V_g characteristics with the evaluated ultralow current characteristics. Figure 13 summarized gate leakage current characteristics both at on-state and off-state obtained from Fig. 9 and Fig. 12. In the voltage range of 1.5 V or less ($|V_g| < 1.5 \text{ V}$), it was confirmed that gate leakage current was less than $10^{-20} \text{ A}/\mu\text{m}$ and does not disturb ultralow off-state characteristics. Figure 14 shows a comparison of off-state current characteristics between InZnO Tr. and InGaZnO Tr. No degradation of off-state current was observed in InZnO Tr. down to $10^{-20} \text{ A}/\mu\text{m}$, which is a noise floor level. I_d-V_g curves were confirmed to maintain the subthreshold slope down to $10^{-20} \text{ A}/\mu\text{m}$. S.S. value of InZnO Tr. and InGaZnO Tr. were 66 mV/dec. and 74 mV/dec, respectively. Figure 15(a) and (b) show a trap density calculated from the S.S. values and V_{th} shift under positive gate bias temperature stress, respectively. InZnO Tr. showed an excellent reliability, which may result from improved interface and channel of InZnO.

Conclusion

We have demonstrated and verified the advantages of InZnO channel compared to InGaZnO. In addition to higher mobility ($>30 \text{ cm}^2/\text{Vs}$), InZnO Tr. showed a lower R_{para} and suppressed gate leakage current at on-state. Moreover, ultralow ($<10^{-20} \text{ A}/\mu\text{m}$) off leakage current characteristics were confirmed to maintain even though EOT scaling down to 6.2 nm.

References: [1] K. Nomura et al., Nature, 432, 488 (2004), [2] T. Aoki et al., ISSCC 2014, p502, [3] S H. Wu et al., VLSI 2016, p58, [4] J. B. Ko et al., IEEE Electron Device Lett., 37, 39 (2016), [5] S. Tomai, et al., J. J. Appl. Phys., 51 03CB01 (2012), [6] W. Li et al., App. Phys. Lett., 107, 063504 (2015), [7] D. H. Lee, et al., IEEE Electron Device Lett., 32, 1695 (2011), [8] A. Takagi et al., Thin Solid Films, 486, 38 (2005).

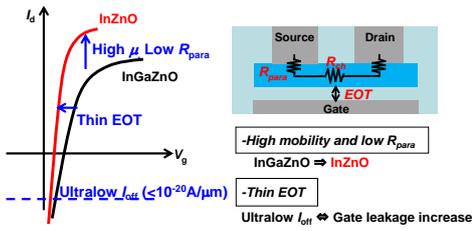


Fig. 1 Concept of high-performance OS Tr. with high I_{on} and ultralow I_{off} . InZnO Tr. was found to show not only higher mobility but lower R_{para} than InGaZnO Tr. In order to maintaining ultralow I_{off} , EOT was carefully scaled down by evaluating ultralow gate leakage characteristics.

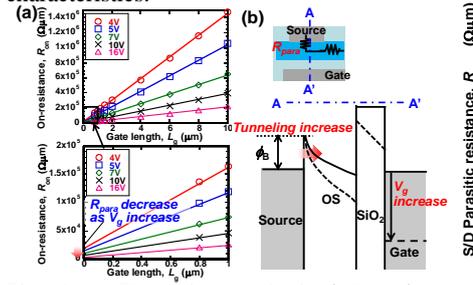


Fig. 4 (a) Extraction method of R_{para} from Fig. 5 R_{on} - L_g plot and (b) schematic illustration of between InZnO Tr. and InGaZnO Tr.

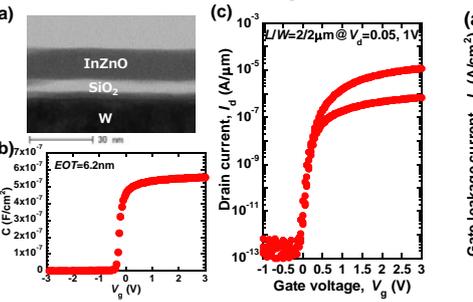


Fig. 5 Comparison of R_{para} between InZnO Tr. and InGaZnO Tr.

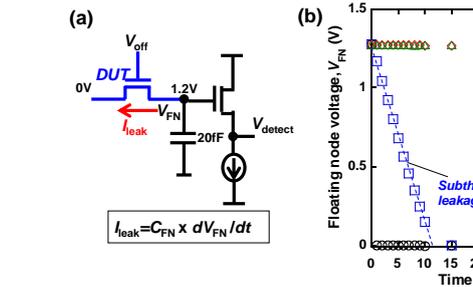


Fig. 6 Extraction of effective SBH from R_{para} at small $V_g - V_{th}$ region.

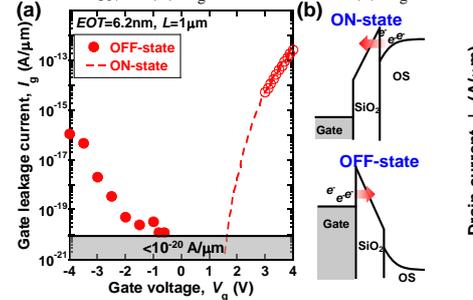


Fig. 7 I_{on} improvement by L_g scaling calculated from extracted mobility and R_{para} .



Fig. 8 (a) TEM image, (b) C - V and (c) I_d - V_g characteristics of InZnO Tr. with EOT of 6.2 nm.

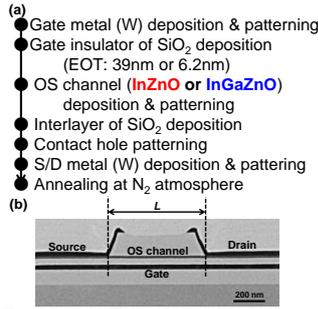


Fig. 9 (a) I_d - V_g characteristics of InZnO Tr. and InGaZnO Tr. at on-state and (b) Fowler-Nordheim plot.

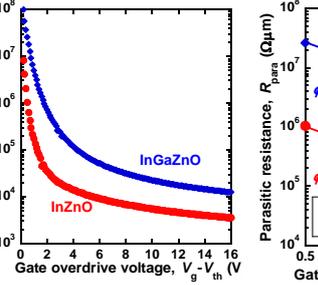


Fig. 10 Schematic band diagram of InGaZnO and InZnO. E_c of InZnO was estimated to be lower than that of InGaZnO, which may contribute to the decreases of R_{para} and on-state gate leakage current.

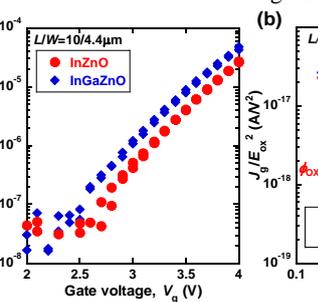


Fig. 11 (a) Circuit diagram of ultralow leakage current measurement and time dependence of V_{FN} at (b) $V_g = 0 \sim 0.4$ V and (c) $V_g = -2$ V.

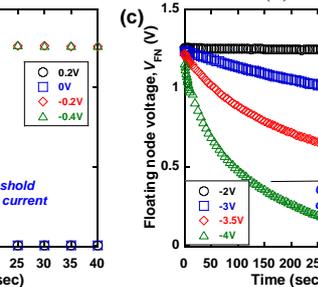


Fig. 12 Obtained off leakage current characteristics with EOT of 6.2 nm.

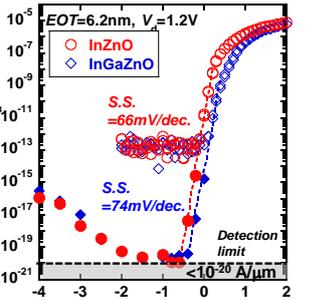


Fig. 13 (a) I_g - V_g characteristics at on-state and off-state and (b) schematic illustration of gate leakage current in OS Tr.



Fig. 14 Comparison of I_d - V_g characteristics between InZnO Tr. and InGaZnO Tr.

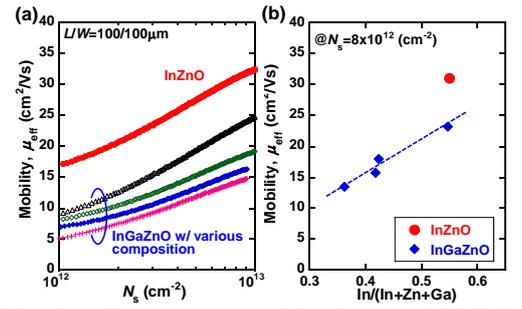


Fig. 15 (a) Comparison of trap density estimated from $S.S.$ values and (b) V_{th} shift under positive gate bias temperature stress.

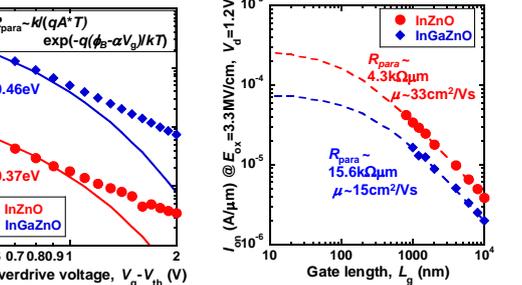


Fig. 16 Comparison of mobility between InZnO Tr. and InGaZnO Tr. and (b) In composition ratio dependence of mobility.

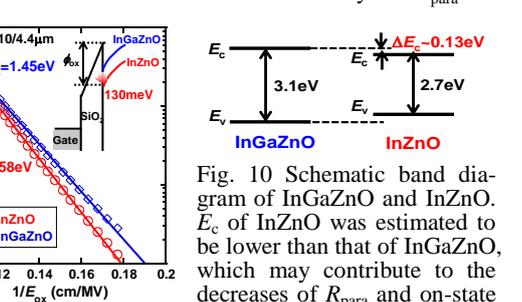


Fig. 17 I_{on} improvement by L_g scaling calculated from extracted mobility and R_{para} .

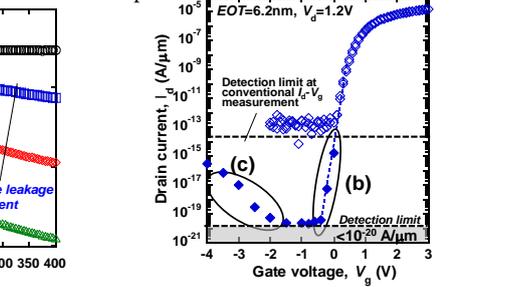


Fig. 18 Comparison of I_d - V_g characteristics between InZnO Tr. and InGaZnO Tr.

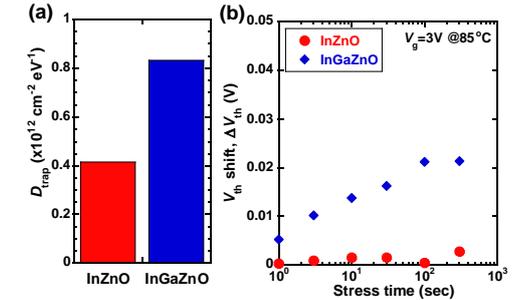


Fig. 19 Comparison of trap density estimated from $S.S.$ values and V_{th} shift under positive gate bias temperature stress.