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1TFT-1RRAM Cell on Polymeric Substrate as Non-Volatile Memory Element Enabling Future Flexible Electronic Platforms

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Abstract

We present a route for monolithic integration of a self-aligned amorphous InGaZnO thin-film transistor (TFT) with a TaOx non-volatile resistive switching memory element (RRAM) on a flexible polymer substrate. The integrated 1TFT-1RRAM memory cell is shown to cycle 165 times with mean memory window of 7.7.

1. Introduction

Flexible electronics is a relatively young discipline compared to the standard electronics developed on monocrystalline silicon substrates. Nonetheless, in recent years, flexible electronics has experienced many advancements, especially in areas where the intrinsic rigidity and size of Si chips impede their use. Metal-oxide thin-film transistors (TFTs) are amenable to direct fabrication on polyimide (PI) as flexible substrate. This technology has received significant attention for displays, large-area imagers and radio frequency identification smart tags [1, 2, 3]. Still, a reliable non-volatile memory component which is electrically re-programmable at low voltage and simultaneously integrated with flexible TFTs has not yet become a standard, even though many concepts have been proposed [4].

This work elaborates on the direct integration of 1TFT-1Resistive Random Access Memory (RRAM) cells on flexible polymeric substrate and presents the memory characteristics of fabricated devices. In this arrangement, the RRAM is the element responsible for memory properties while the transistor is used as a select and a current-limiting element. Arrays of such type of memory cells are envisioned to realize large memory blocks integrated closely to TFT circuits for future flexible applications. However, direct fabrication of a complete device on top of a polymer substrate brings various technology challenges which are addressed in this work by careful design layout and optimized fabrication.

2. Monolithic TFT-RRAM integration route

The standard fabrication process for self-aligned TFTs based on amorphous InGaZnO consists of four photolithography steps, namely semiconductor, gate, S-D via and S-D metal patterning. This TFT architecture is advantageous in terms of parasitic wire capacitances due to the non-overlapping gate/S-D contacts. We propose in this work to include three additional photolithography mask steps to monolithically integrate an RRAM element with the InGaZnO self-aligned TFT: one to define the memory cell via, starting from the gate metal, a second mask to pattern the memory layer and the third to define the routing metal. The cross-section of the 1TFT-1RRAM integration along with the corresponding mask set are depicted in Fig. 1 (a). The entire stack is fabricated at low temperatures (≤ 350 ºC) directly on top of the flexible PI substrate. This flexible foil is temporarily mounted on the carrier substrate which keeps it mechanically stable during fabrication. As previously mentioned, the selected semiconductor material in this work is InGaZnO, the gate metal which simultaneously serves as one of the RRAM electrodes is made of MoCr, while the RRAM material is based on TaOx metal-oxide. For routing purposes, low sheet-resistance Ti/Al/Ti was used for both the S-D and routing metal layer. Critical dimension of both devices amounts to 5 µm, namely the transistor minimal channel length and size of the RRAM via. Fig. 1 (b) depicts a microscope image of the final 1TFT-1RRAM integration after completion of process flow.

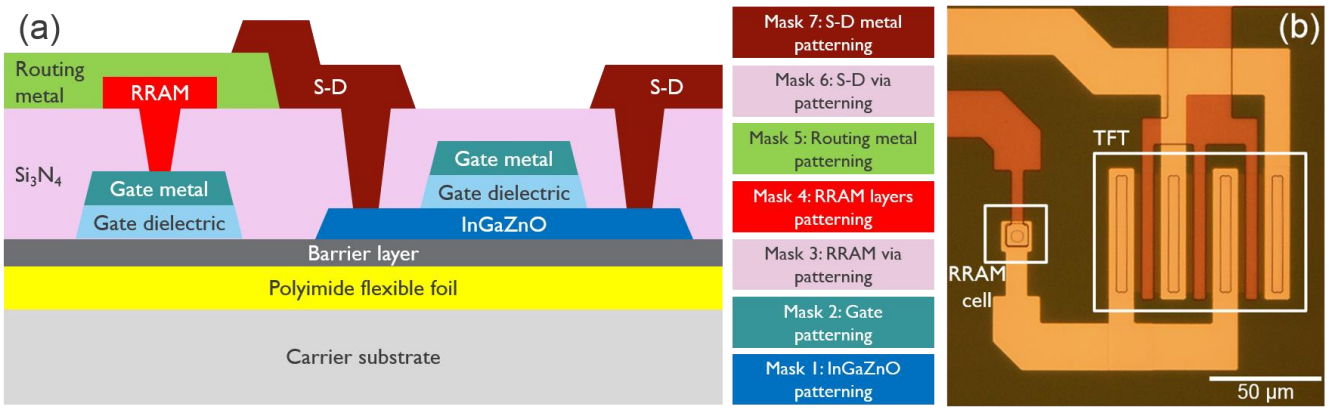

Figure 1. (a) Cross-section and mask set of TFT-RRAM device, (b) TFT-RRAM integration under 50x magnification

3. Measurement results

Fig. 2 shows the measured transfer characteristics of various TFT sizes. These characteristics present the average value of 70 devices of each size over different wafer positions. As the transistor channel increases, the maximum obtainable current increases as well, resulting in an increase from ~ 190 µA for W = 250 µm to ~ 720 µA for W = 1000 µm taken at V_{GS} = 5 V and V_{DS} = 5 V. Inset of Fig. 2 plots statistical distribution of maximum currents for different TFT sizes. The resulting threshold voltage of fabricated transistors has a negative mean value of V_{TH} = -0.3 V with standard deviation of 150 mV.

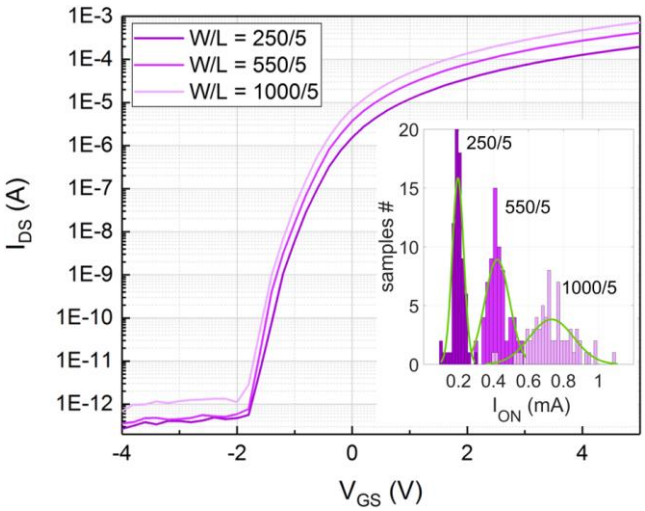

Figure 2. TFT transfer characteristics for different TFT sizes: W/L = 250/5, W/L = 550/5, W/L = 1000/5

Subsequently, the characterization of the 1TFT-1RRAM integrated cells was performed. RRAM in its pristine state is non-conductive. To initialize the memory cell, a single forming step by means of a voltage bias over the RRAM element is performed creating conductive filament through the memory metal-oxide, thus bringing the cell into the conductive state (Fig. 3).

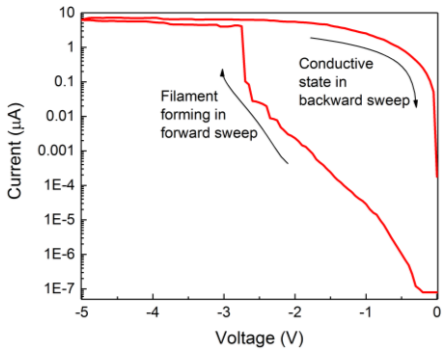

Figure 3. RRAM forming

Later, the cell is continuously switched between high-conductive and low-conductive states through series of reset and set voltage sweeps that quench and open previously formed conductive filament (Fig. 4). These voltage sweeps have opposite polarity for the reset compared to the set process and are applied to the RRAM electrode corresponding to the gate metal in Fig. 1 (a). The source contact of the TFT is kept grounded during these measurements while its gate contact had a constant bias of V_G = 5V. The obtained memory window (MW) which quantitatively describes the ratio between the two memory states amounts to 7.7 measured at 0.5 V for an average over 165 consecutive cycles. The size of the measured memory element is 5 µm x 5 µm, while the selected TFT size is W/L = 700/5. A MW larger than 7 persists in a wide read-out voltage range which allows a reduced precision of the read-out electronics.

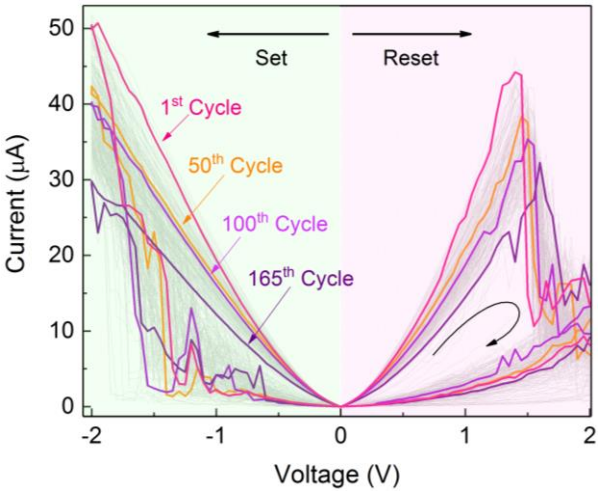

Figure 4. TFT-RRAM switching characteristics based on 165 cycles

4. Conclusion

This work presents a successful monolithic integration of a 1TFT-1RRAM cell using low-temperature fabrication on top of a flexible PI substrate. TaOx based RRAM cells are combined with a self-aligned InGaZnO TFT in a single process flow thanks to specifically developed design and stack architecture. 165 set/reset cycles have been successfully demonstrated for 1TFT-1RRAM cell with a mean memory window of 7.7, paving the way for integration of such non-volatile memory blocks in various flexible electronics applications.

Acknowledgements

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References

[1] J. S. Yoon *et al.*, "55-inch OLED TV using optimal driving method for large-size panel based on InGaZnO TFTs," *Dig. Tech. Pap. - SID Int. Symp.*, vol. 45, no. 1, pp. 849–852, 2014.

[2] C. Zhao, and J. Kanicki, "Amorphous In-Ga-Zn-O thin-film transistor active pixel sensor x-ray imager for digital breast tomosynthesis," *Med. Phys.*, vol. 41, no. 9, p. 91902, 2014.

[3] K. Myny, "The development of flexible integrated circuits based on thin-film transistors," *Nat. Electron.*, vol. 1, no. 1, pp. 30–39, 2018.

[4] M. Ghoneim and M. Hussain, "Review on Physically Flexible Nonvolatile Memory for Internet of Everything Electronics," *Electronics*, vol. 4, no. 3, pp. 424–479, 2015.