Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp589-590

# 1T Linear-Log Response Pixel Sensor in 28nm FDSOI Technology

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**Abstract**

**We demonstrate a 1T pixel sensor in 28nm FDSOI technology that exhibits two responses: logarithmic at high intensities and linear at low intensities to improve performance under low illumination. The reset is performed using the back gate of the FDSOI and can be commonly applied to all pixels, enabling very small pixel size. By optimizing the integration time and the pixel dimensions, the sensitivity in linear regime reaches 2.33mV/lux.s and the overall dynamic range is 120-130dB.**

## 1. Introduction

Standard image sensors with a linear response have a very good low light sensitivity but suffer from a low Dynamic range (DR) (3-4 decades). One of the most promising techniques to extend DR is the logarithmic image sensor [1]. However, its high power consumption, and poor sensitivity at low light are major drawbacks. To improve low-light performance while keeping a high DR, sensors combining both linear and log response have been proposed [2-4]. The DR range is extended, but at the expense of adding transistors per pixel. We previously demonstrated a pixel sensor that contains only one transistor/pixel based on the back bias effect in FDSOI technology [5]. In this paper, we demonstrate that the 1T FDSOI pixel can be used as a linear-log sensor without additional transistors. Both lin and log regions of operation can be optimized for dedicated applications, while keeping a very small footprint. An analytical model is developed based on Leti's UTSOI model [6] and JUNCAP model [7], allowing pixel optimization using SPICE simulations. The results are confirmed experimentally by opto-electrical characterizations.

## 2. Pixel structure and operation

The pixel consists in an FDSOI transistor (Fig.1.), N- or P-MOS, where a photodiode has been implemented under the buried oxide (BOX). By modifying the Well ion implantation step in the standard FDSOI process flow, the photodiode is obtained without additional masks nor change in the integration flow [5]. The light incident on the device generates electron-hole pairs that are separated by the diode electric field, and accumulates at the BOX-GP (ground plane) interface. The accumulation of charges modifies the potential of the GP, and due to a capacitive coupling with the channel, it will result in a Light Induced $V_T$ Shift (LIVS) (Fig.2.). Fig.3 shows the measured transient response of the device to a light pulse, where the long decay time (>10s) reflects the low leakage current of the photodiode. In DC regime, the LIVS exhibits a logarithmic response over 8 decades of optical power ($P_{OPT}$) (Fig.4). The LIVS is optimized by using different capacitive coupling coefficients.

To reset the pixel, the bulk voltage (Well) is used, avoiding the use of an extra transistor. For the tested NMOS transistor with a BOX/PN oriented junction, the diode is first forward biased by applying a negative pulse on the well to charge the diode capacitance. After the reset pulse, a certain amount of charges are stored in the GP, inducing a potential that reverse bias the diode. The value of the induced potential is defined by a capacitive divider that takes place across the structure as shown in Fig.5, and thus depends on the device geometry. Using SPICE simulation, the reset is proven to be effective: as shown in Fig.6, the same current level is achieved after the reset pulse, whatever the initial light intensity.

Opto-electrical characterization are performed in both DC and transient mode, using a wide band visible spectrum and front side illumination. The DC consists in $I_DV_G$ curves at different intensities to measure the LIVS response to $P_{OPT}$. As can be seen in Fig. 7, there is good agreement between experimental results and SPICE simulation among the experimental light source intensities available. For the transient test, the NMOS is biased in subthreshold regime at $V_G$=0.38V and $V_{DS}$=0.9V, the integration time is 20ms, and the reset pulse is -2V. After integration the current is measured and converted to an LIVS through the subthreshold swing of the NMOS, to compare the response with the DC case.

## 3. Regions of operations

From the performed measurements (Fig. 8), two regions of operation are identified: linear response for lower intensities and log response for higher intensities where the diode is reverse biased (charge integration Fig.9) and weakly forward biased (charge accumulation Fig.10). After the reset pulse, the potential of the diode decreases at a rate depending on light intensity, until it reaches its short circuit current (Isc) (Fig. 9). Passing the Isc, the charges starts to accumulate and the voltage on the diode corresponds to the open circuit voltage (Voc) (Fig. 10). As the Voc has a logarithmic dependence on the photocurrent (Iph), the response becomes logarithmic with respect to $P_{OPT}$. As summarized in Table 1 using SPICE and TCAD simulations, optimized DR and sensitivity values are estimated to be around 120-130dB and 8-11.6mV/dec respectively. In this case, the integration time (Fig. 11) and the device architecture (example in Fig. 12) are adapted to extend the DR of the linear response.

## 5. Conclusion

In this work, we demonstrate a 1T pixel sensor in FDSOI technology standard process capable of operating in two regimes, linear and log without changing the circuitry. The reset is performed using the bulk voltage, and the integration time is adapted to optimize the overall response depending on the application. We also show that the sensitivity is enhanced by properly engineering the structure capacitances. This work

opens the path for low power, small pitch, monolithically integrated FDSOI CMOS 1T lin-log response pixels.

## References


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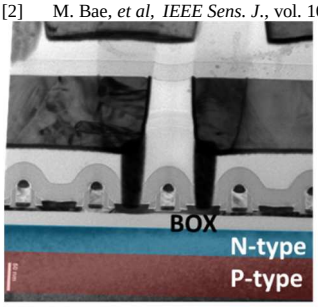


Fig 1: TEM imageof FDSOI + diode structure. L=30nm, $T_{BOX}$=25nm

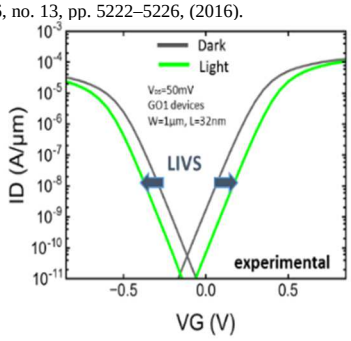


Fig 2: NMOS and PMOS transistor $I_{D\text{-}rain}$ vs $V_{GS}$ with and without light illumination. Light induced VT shift is observed.

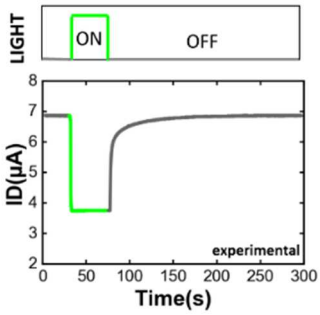


Fig 3: transient characteristics of the NMOS/NP when a light pulse is applied. Transient >10s indicate low diode leakage current

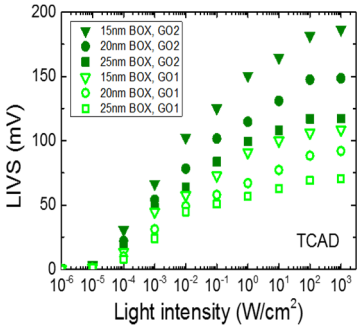


Fig.4 LIVS in mV vs optical power in W/cm² for different capacitive coupling coefficient by varying $T_{BOX}$ and $T_{OX}$.

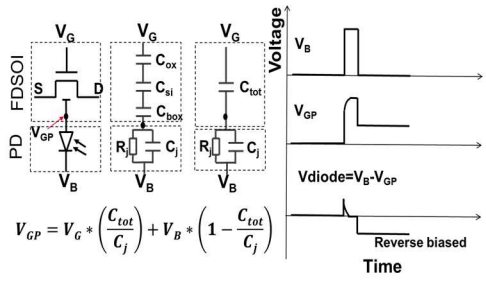


Fig 5: FDSOI +Diode capacitance equivalent circuit and capacitive divider for applied pulse on bulk (Well) illustrating reset concept

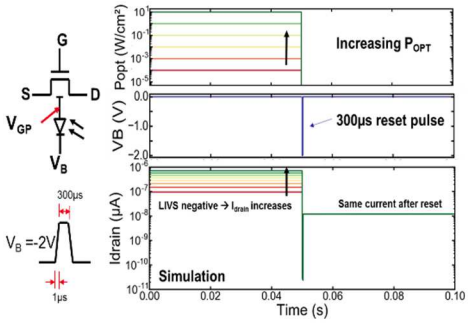


Fig 6: NMOS/PN diode reset operation by applying a pulse on $V_B$. The current level is the same whatever the initial light intensity. Tpulse=300µs, Vrst=-2V

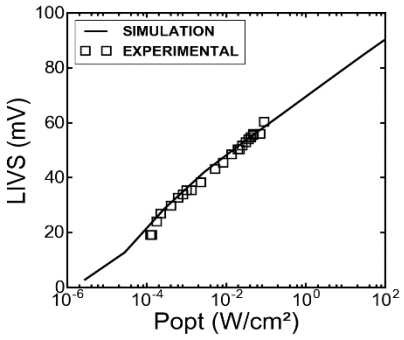


Fig 7: NMOS/PN LIVS vs $P_{OPT}$ experimental results vs SPICE simulations

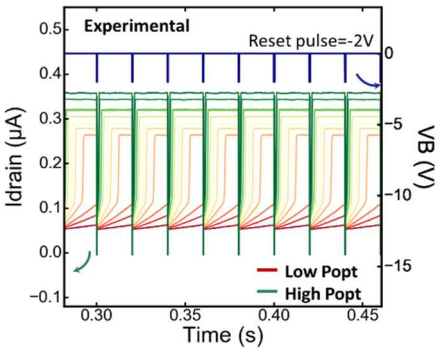


Fig 8: Reset validation for NMOS/PN device at different constant light intensities. $V_B$=-2V, VG=0.38V, VDS=0.9V, Tint=20ms. L=W=2µm

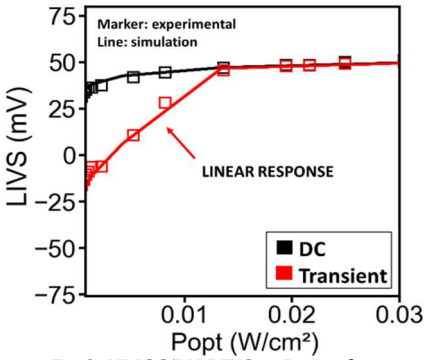


Fig 9: NMOS/PN LIVS vs $P_{OPT}$ in linear showing the linear regime (integration mode)

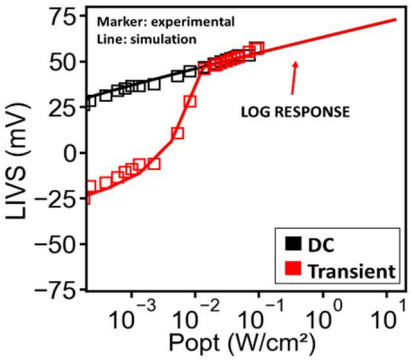


Fig 10: NMOS/PN LIVS vs $P_{OPT}$ in log scale showing the log regime (accumulation mode)

| | | Sensitivity | | DR | |
|---|---|---|---|---|---|
| | | Lin (mV/lux.s) | Log (mV/dec) | Lin (dB) | Log (dB) |
| TBOX(nm) | 25 | 1.7 | 8.12 | 48 | 67 |
| | 15 | 2.05 | 10.5 | 52 | 65 |
| | 10 | 2.33 | 11.62 | 55.5 | 61 |
| Tint(ms) | 10 | 0.8318 | 8.12 | 55 | 65 |
| | 20 | 1.66 | 8.12 | 48 | 72 |
| | 30 | 2.54 | 8.12 | 44 | 76 |

Table 1: Pixel linear and log regions sensitivity and DR comparison for different Tint and TBOX

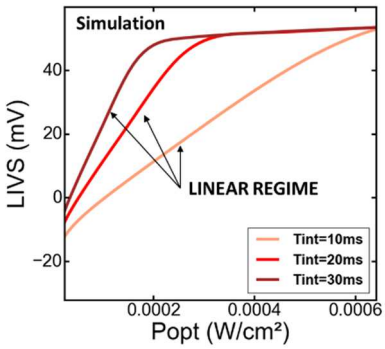


Fig 11: NMOS/PN LIVS vs $P_{OPT}$ for different integration time.

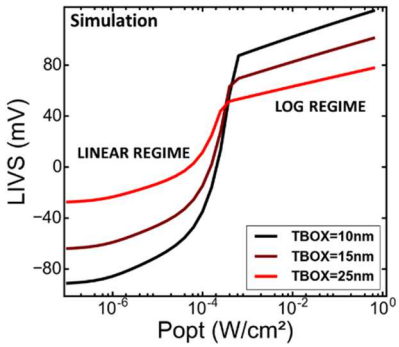


Fig 12: LIVS vs $P_{OPT}$ for different $T_{BOX}$.


## Acknowledgment

The authors thank STMicroelectronics for partial processing of the wafers in Crolles facilities