A 3.4µm Pixel Pitch Global Shutter CMOS Image Sensor Over 110dB Dynamic Range in One-Frame Exposure with Dual In-Pixel Charge Domain Memory

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Abstract

A newly developed 3.4µm pixel pitch global shutter CMOS image sensor (CIS) with dual in-pixel charge domain memory (CDMEM) has about 5.3M pixels and achieves 19ke- full well capacity and 30ke-/lx·s sensitivity.

Furthermore, this image sensor realizes various readout with dual CDMEM. For example, an alternate multiple accumulation high dynamic range (HDR) readout procedure achieves over 110dB dynamic range in one frame operation and is suitable in particular for moving object capturing. This front-side-illuminated CIS is fabricated in a 130nm 1P4M with light shield CMOS process.

1. Introduction

CMOS image sensors (CISs) with global shutter (GS) function are required in a variety of application areas, including machine vision, automobile and surveillance. For these applications, GS CISs are demanded high image quality (e.g., high full well capacity (FWC), high sensitivity) in addition to image accuracy (e.g., simultaneity) to avoid rolling shutter distortion. These applications also benefit from the high dynamic range (HDR), high framerate (HFR) and high-image quality video capturing (e.g., low jerkiness degradation).

A charge domain memory (CDMEM) is advantageous in low kTC noise with correlated double sampling (CDS) for a floating diffusion (FD) based GS [1] and a voltage domain memory (VDMEM) [2, 3], although, is disadvantageous in fill factor and parasitic light sensitivity (PLS).

Dual CDMEM realizes various readout procedures, instead of an additional memory and transfer gates. For example, by transferring the short exposure signal and the long exposure signal to dual memory alternately, the HDR readout suitable for moving object capturing is realized.

2. Sensor Architecture

Fig. 1 shows a block diagram of the GS sensor. The chip comprises a pixel array (2676H×2200V) and column 10b SSDG-ADC (12b equivalent) [4]. Fig. 1 also shows a schematic diagram of the pixel. A unit pixel consists of a two-FD shared and with dual in-pixel CDMEMs (MEM), respectively.

Fig. 2(a) shows a binning readout mode with multiple accumulation (ACC) shutter [4]. In this mode, dual CDMEM work as one CDMEM by simultaneous transfer with GS and TX. The pixel FWC is the summation of two CDMEM FWC. Fig. 2(b) shows a HFR readout mode with multiple ACC shutter. In this mode, dual CDMEM work two frames in turn and output signal, respectively. The framerate becomes faster in spite of the FWC decrease to one CDMEM FWC.

3. Pixel Performance and Application

Fig. 3 shows a chip package photograph and Table I summarizes the CIS characteristics. FWC is 9.5ke- in 120fps HFR mode and 19ke- in 100fps binning mode, respectively. In addition, sensitivity, temporal noise and PLS are 30ke-/lx·s, 2.8e-rms and -83dB, respectively.

Fig. 4(a) and 4(b) show a conventional single ACC HDR with one CDMEM and a suggested alternate multiple ACC HDR with dual CDMEM. In suggested readout, the short exposure and the long exposure are divided in some blocks, and are performed alternately. Furthermore, the accumulated signal charges are divided into dual CDMEM, alternately, and are transferred, respectively. In Fig. 4(a) and 4(b), total exposure time is identical. The short exposure is $115\mu s (23\mu s \times 5)$ and long exposure is $14.7ms (3.68ms \times 4, 115\mu s \times 128)$.

Fig. 5 shows remarked area images before and after the image synthesis. In Fig. 5, the single long result is almost same as alternate multiple ACC long result, therefore it is omitted. Resolution lost in the halation area of the long ACC and the blackout area of the short ACC are restored in the HDR image. In the conventional single ACC HDR, the moving LED is synthesized unnaturally. This is because ACC timing is not identical between the short exposure and the long exposure. By using alternate multiple ACC, the moving LED is synthesized naturally. Particularly, in video image, the jerkiness degradation is well suppressed.

Fig. 6 shows a whole synthesized image. We allocated about 8dB overlap for the stitching point to be hardly noticeable. As a result, the dynamic range increases from 77dB with the binning readout procedure (Fig. 4(a)) to 111dB.

4. Summary and Conclusion

Table II lists the performance comparison of recently published CISs [1-6]. Based on recent results, several characteristics are comparable or better than those of others, in spite of the pixel size shrinkage, the front side illuminated structure and the addition of the CDMEM and transfer gates.

A 3.4µm pixel pitch global shutter CMOS image sensor with dual in-pixel charge domain memory is developed. The sensor achieves over 110dB dynamic range in one-frame exposure with alternate multiple ACC. This ACC is applicable even to moving objects capturing.

References

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Fig. 1: CIS block and the pixel schematic diagram



Fig. 2: Binning and HFR signal readout procedure



Table I: Chip characteristics

2/3 inch

3.4 µm

2592 (H) x 2054 (V)

Binning

100 fps

19000 e

30000 e-/lx·s

2.8 e*ms

77 dB

-83 dB

HDR

60 fps 940000 6

(Equivale

111 dB

Fig. 3: Chip-package photograph







Fig. 5: Remarked area images before & after synthesis



Fig. 6: Synthesized HDR image (60fps, 14.8ms ACC, F4)

Table II : <u>Performance comparison</u>	of recently	CISs
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	This work	[1]	[2]	[3]	[4]	[5]	[6]
Shutter Function Storage Node	GS 2CDMEM	GS FD	GS 2VDMEM	GS VDMEM	GS CDMEM	GS CDMEM	GS CDMEM
Pixel Pitch [µm]	3.4	4.8	3.75	4.6	3.4	3.875	5.6
Num. of Eff. Pixels	5.3M	4.1M	0.8M	47.6M	5.3M	1.3M	1.1M
Max. Frame Rate [fps]	120	280	50	30	120	N/A	21
Full Well Capacity [e-] (per pixel area) [/µm ²]	19000 (1640)	N/A	8100 (580)	14600 (690)	16200 (1400)	224000 (14900)	6800 (220)
Sensitivity [e-/lx·s] (per pixel area) [/µm²]	30000 (2590)	28400 (1230)	N/A	N/A	28000 (2420)	36200 (2410)	N/A
Temporal Noise [e-ms]	2.8	4.2	8.5	8.8	1.8	N/A	0.61
Dynamic Range [dB] HDR mode [dB]	77 111	N/A	59 102	65 -	79 111	N/A 88	81 -
PLS [dB]	-83	N/A	-80	-85	-89	-83	-60