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A 125Mfps Global Shutter CMOS Image Sensor with Burst Correlated Double Sampling during Photo-Electrons Collection

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Abstract

This paper presents an ultra-high speed (UHS) global shutter CMOS image sensor (CIS) with pixel-wise analog memory array achieving the frame period of photo-electrons transit time by burst correlated double sampling (CDS). The fabricated chip prototyping a 3D stacked structure with 34.56μm pitch equivalent pixels achieved 8ns frame period, resulting in 100M frames per second (fps) with 80 recording frames (record length) and 125Mfps with 40 record length under room temperature without any cooling systems.

1. Introduction

In order to meet the demands on visualizing ultra-high speed phenomena in scientific, engineering, medical fields and so on, R&Ds of UHS image sensors toward over 100Mfps and highly time-resolved image sensors have been actively conducted[1-10].

Figure 1 shows the limiting factors of frame rate in CIS[4]. By an introduction of on-chip analog memories, the factors (D) and (E) were eliminated, and 10Mfps with 100kpixels and 128 record length has been achieved[3,6]. Utilizing the 3D stacking technology with pixel-wise connections between the two substrates[11-12], it is theoretically investigated that the factors (B) and (C) are reduced significantly[13]. Recently a CIS with analog memory array placed closely to each pixel has been reported to exhibit 71.4Mfps[14]. The ultimate frame rate or time resolution of image sensors is limited by the factor (A): the photo-electrons transit time in photodiode (PD)[9-10,15].

In this work, we demonstrate an UHS CIS with pixel-wise analog memory array that operates global shutter burst CDS with minimized pulse transitions at the floating diffusion (FD) connected to the high speed charge collection pinned PD. It achieves the frame period of photo-electrons transit time. A planar-type CIS with $25^{H}\times100^{V}$ pixels with 80 analog memories/pixel toward the 3D stacked structure shown in Fig.2 was designed and fabricated by a 0.18μm 1-poly-Si 5-Metal technology and its performance was measured under the room temperature condition without any cooling systems.

2. Developed Image Sensor Structure and Operation

Fig.3 depicts the block diagram of the developed CIS shown on the fabricated chip micrograph. It consists of the array of pixels and pixel-wise analog memories, memory select circuit, vertical and horizontal scan circuits for signal outputting from memory array, and output buffers. The pixel arrangement in this work is illustrated in Fig.2(a). It is a prototype of the final structure shown in Fig.2(b) with backside illumination 3D stacking technology with pixel-wise connections.

Fig.4 shows the pixel circuit schematic. It consists of a $30.00\times21.34\mu m^2$ high speed charge collection pinned PD using dopant concentration gradient and fringe electric field[16] directly connected to a FD without a transfer gate, a reset switch (R), a source follower (SF1), a select switch (X), a current source (CS1), CDS bypass/select switches, a CDS circuit with a SF buffer (SF2), a 1T1C-type analog memory array with column signal line switches and memory readout circuit comprised of SF buffer. The number of analog memories in this work is 80 in 34.56μm pitch area using MOS capacitors, and it can be increased to about 400 by introducing the $30fF/\mu m^2$ vertical trench capacitors[7]. The developed chip operates in two modes: in-pixel and off-pixel burst CDS modes with record length of 80 and 40, respectively.

Fig.5 shows the pixel layout diagram with metal wiring arrangement for (a) this work and (b) previous works[3,6]. In this work, the signal output line is fully pixel-parallel and it is shortened from about 8mm in previous works to about 40μm. The width and space of metal wires for pixel driving and memory select pulses laid horizontally are relaxed to shorten RC time constant. These contribute to minimize the limiting factors (B) and (C) in Fig.1. Also, SF3 buffers are eliminated to reduce the current consumption during video capturing.

Fig. 6 shows the timing and pixel potential diagrams of the introduced burst CDS operation with minimized pulse transitions. First, PD and FD are reset and the reset noise (V_N) appears at t_1, then the first signal comprised of $V_{sig1}+V_N$ are readout at t_2 for noise cancelling. After the integration period the second signal comprised of $V_{sig2}+V_N$ are readout at t_3. In the off-pixel burst CDS mode, the frame period is reduced to 8ns, reaching the photo-electrons transit time in the large PD.

3. Chip Fabrication and Measurement Results

The prototype chip with $25^{H}\times100^{V}$ pixels with 80 analog memories/pixel was fabricated by a 0.18μm 1-poly-Si 5-Metal technology. The supply voltage is 3.3V. Fig.7 shows the current consumption/pixel during video capturing. By eliminating SF3 buffers and reducing current values, the current consumption was reduced from 210μA in the previous work[6] to 86μA and 50μA in the in-pixel and off-pixel burst CDS modes, respectively. The smaller current is advantageous when increasing the number of pixels. Fig.8 show the measured frame rate as a function of record length with other works[1-8, 14]. By the introduction of the burst CDS operation with shortened signal output lines, 100Mfps and 125Mfps were achieved by in-pixel CDS and off-pixel CDS modes, respectively. Fig.9 shows the sample video capturing system and the captured images at various frame rates. Good image quality up to 125Mfps was successfully confirmed without any cooling systems. Table I summarizes the chip performance.

4. Conclusion

An UHS global shutter CIS with pixel-wise memory array reaching the frame period of photo-electrons transit time by the burst CDS operation was developed. The prototype sensor chip toward the backside-illuminated 3D stacked structure with 34.56μm pitch equivalent $25^{H}\times100^{V}$ pixels exhibited 100Mfps with 80 record length and 125Mfps with 40 record length without any cooling systems.

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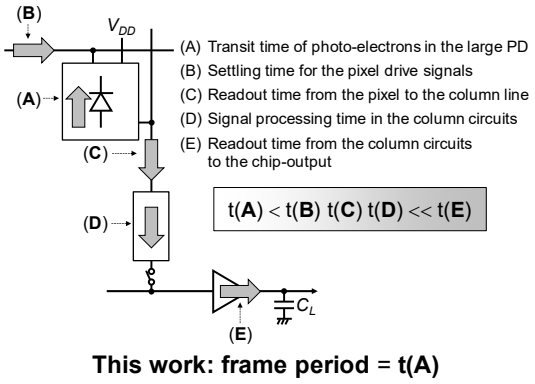

Fig. 1 Limiting factors of frame rate in CMOS image sensors.

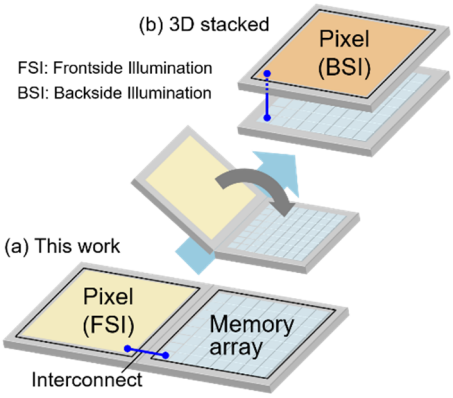

Fig. 2 Conceptual illustrations of pixel arrangement of (a) this work and (b) 3D stacked chip.

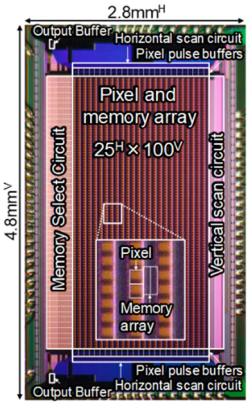

Fig. 3 Chip micrograph and block diagram.

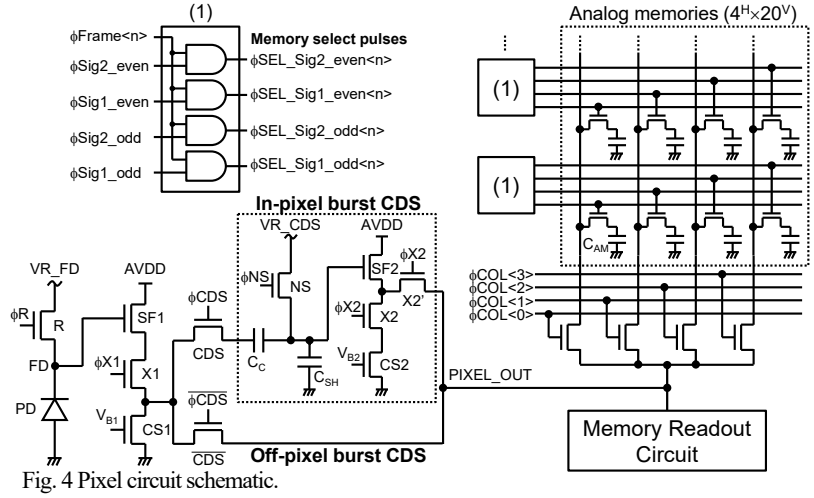

Fig. 4 Pixel circuit schematic.

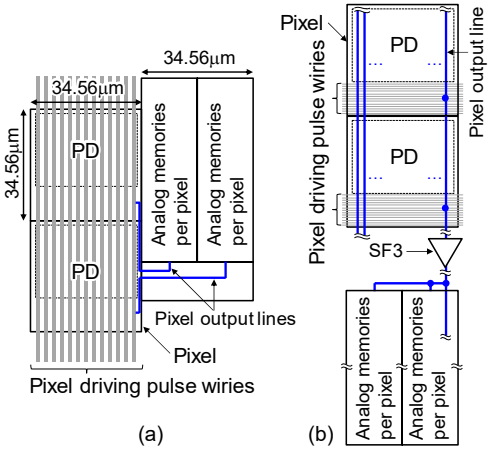

Fig. 5 Pixel layout diagram of (a) this work and (b) previous works[3,6].

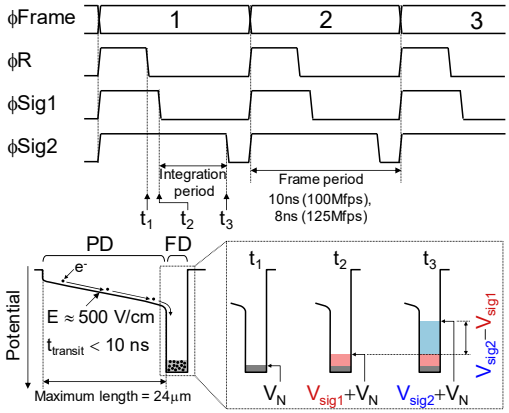

Fig. 6 Pulse timing diagram of burst CDS and pixel potential diagram.

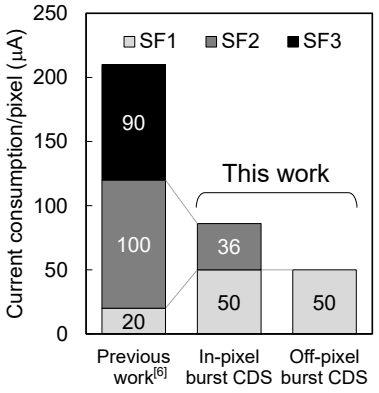

Fig. 7 Current consumption/pixel during video capturing.

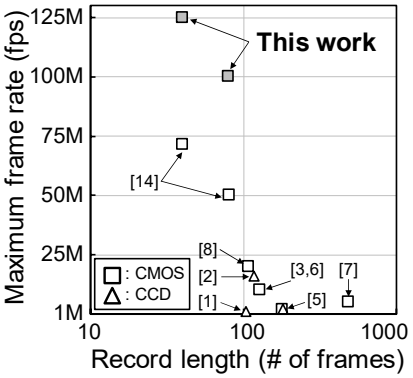

Fig. 8 Frame rate as a function of record length.

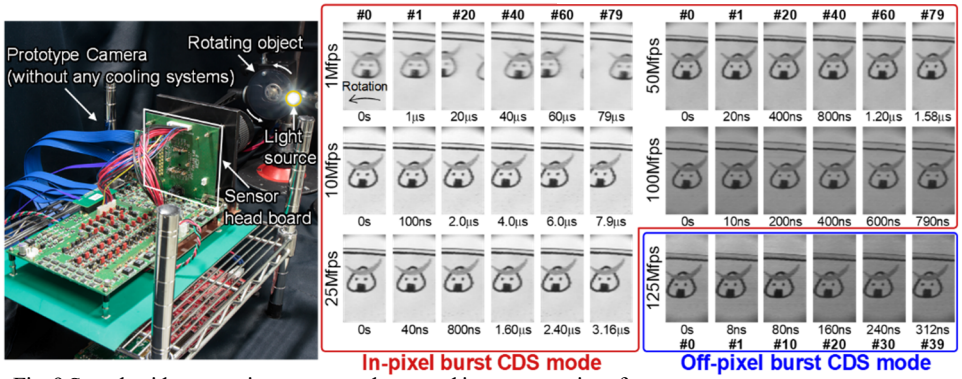

Fig. 9 Sample video capturing system and captured images at various frame rate.

Table I
Performance Summary.

Technology	1P5M 0.18 μm CMOS	
Supply voltage [V]	3.3	
Pixel pitch [μm] (3D stacking equivalent)	69.12^H × 34.56^V (34.56^H × 34.56^V)	
Photodiode size [μm^2]	30.00^H × 21.34^V	
# of pixels	25^H × 100^V	
# of analog memories /pixel	80	
Maximum frame rate [Mfps]	In-pixel burst CDS mode	Off-pixel burst CDS mode
	100	125
Record length	80	40