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A Built-in Drift-field PD Based 4-tap Lock-in Pixel for Time-of-Flight CMOS Range Image Sensors

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Abstract

This paper presents a 4-tap lock-in pixel with a built-in drift-field PD. A prototype chip has 132 × 84 pixel array, and demonstrates a distance measurement with 4ns light pulse, which is the shortest pulse width among pulse-based TOF range imagers.

1. Introduction

As the demand for time-of-flight (TOF) range imaging has been increasing, numerous TOF range imagers based on CMOS image sensor (CIS) technologies have been presented [1-6]. In the TOF range imagers, a lock-in pixel is a key element because its modulation speed limits an available pulse width or modulation frequency, which determines a range resolution or precision. Multi-tap pixel structure is promising since it is effective for reducing motion artifacts, and improving a range resolution while maintaining a measurable range.

A pinned photodiode (PPD) based lock-in pixels such as a transfer gate modulator [3], and a lateral electric field modulator (LEFM) [4-5] are desired for the better compatibility with a standard CIS technology. In those pixels, however, the unit size of the one modulator is relatively small (~5μm) due to a limited fringing field generated by modulation gates. Since the pixel size of >10 μm is desired in TOF-CISs, the limited unit size leads to a small fill factor or increased gate capacitance due to a parallel connection of modulators.

To overcome this issue, a built-in drift-field (BD) photodiode (PD) based charge modulator has been developed [6]. This is suitable for relatively large pixel size while maintaining high-speed charge modulation. However, this lock-in pixel demonstrates its performance only in relatively slow charge modulation of 30 ns, and it has 3-tap outputs with a drain. In this paper, we have implemented the 4-tap lock-in pixel with draining by using a BD-PD with a cascaded draining and modulating gates. The distance measurement with a very short pulse width of 4 ns is successfully performed, and it demonstrates high range resolution.

2. Proposed Pixel, Operation, and Implementation

Fig.1 shows the proposed modulator layout, cross-sectional views with those potential distributions. The modulator consists of a BD-PD, a modulation diode (MD), four charge modulation gates: G1, G2, G3, and G4. Between the PD and MD, a set of charge draining gates (GDs), is formed. With the GD, photo-charge is controlled to be transferred to charge modulators or discharged to the drain. The BD is created by three n-type layers with different concentrations: n_1, n_2, and n_3. A generated photo-charge in the PD is quickly transferred to the MD with the built-in drift field, and then to a floating diffusion (FD). Since the sensitivity is independent of the MD size, it is designed to be small for enabling a high-speed charge modulation even using a small-sized modulation gate. The small-sized gates have a small load capacitance, which leads to low power consumption as well as high-speed modulation.

Fig. 2 shows a prototype TOF range imager with the proposed modulator. The unit size of the modulator is 11.2 x 11.2 um^2. In the lock-in pixel, 2×2 modulators are implemented in a unit pixel, and those FDs are connected in parallel. The 4-tap pixel outputs are connected in parallel to 4 column ADCs each of which is 5.6 μm pitch. The effective number of pixels is 132 x 84. The gate capacitance is reduced to 20% of the previous work using X-shaped LEFM pixel [5].

Fig.3 shows the timing diagram for 4-tap lock-in pixel with a small duty ratio light pulse. The reflected short light signal is captured by 4 consecutive gate pulses. The G_D is turned on after capturing the signal to suppress the background light. The time of flight (T_d) and the resulting distance is calculated in three time windows (TWs) by the equation shown in Fig.3, where c: velocity of light, T_W: gate width and Q_{13} and Q_{24} are the differences from the first to third, and the second to fourth tapped signal outputs. The measurable range of three TWs is obtained in a single frame.

3. Experimental Results

The prototype chip is implemented in Dongbu HiTek 0.11um 1P4M CIS technology shown in Fig. 4. The pulse width of light and gates are set to 4 ns, which is the shortest in the pulse-based TOF imagers reported [3-6]. The light source is a 850 nm laser. The frame rate is 94 fps.

Fig.5 shows a measured modulation characteristic where offset canceling and a sensitivity correction between the gates is applied. The charge modulation is successfully obtained even at 4 ns light pulse.

Fig.6 shows a measured distance, error, and range resolution under no background light condition. The measured distance is corrected by using a lookup table with linear interpolation. The target is a white flat panel. The good linearity is obtained over 1.0m to 2.7m, the maximum error is approximately 20mm. A high range resolution of 4.2mm at 2.5m is achieved at a power density of 0.12 W/m^2.

3. Conclusions

This paper presents BD-PD based lock-in pixel, of which

prototype demonstrates its high-speed charge modulation capability.

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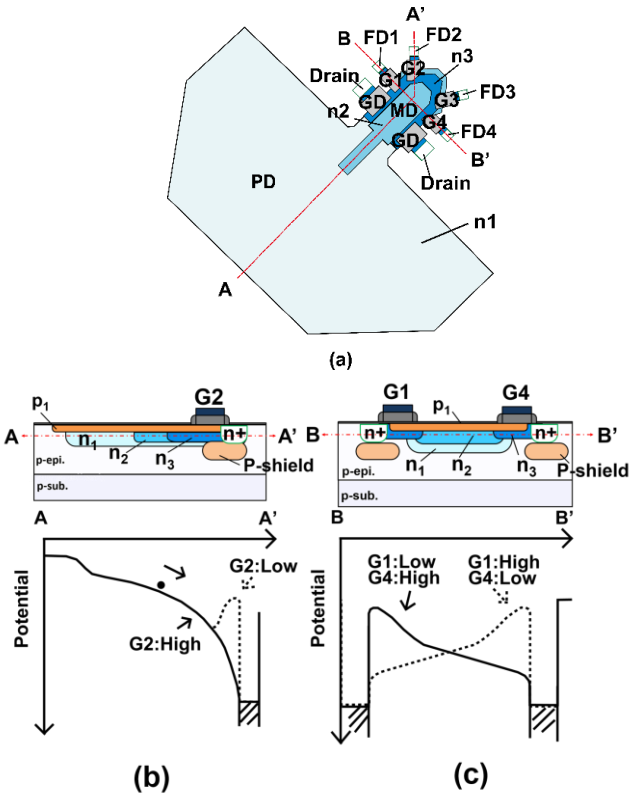

Fig.1 Proposed charge modulator. (a) layout, (b)(c) structure and potential distribution at A-A' , and B-B' axis.

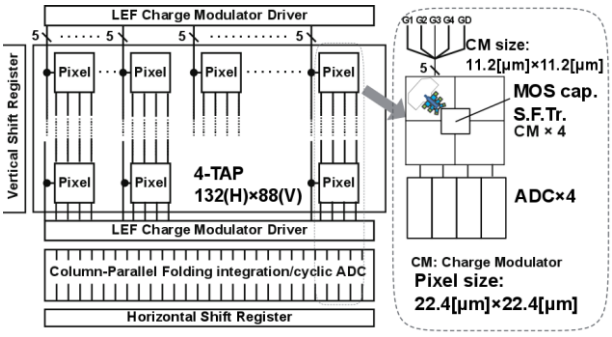

Fig.2 Sensor architecture

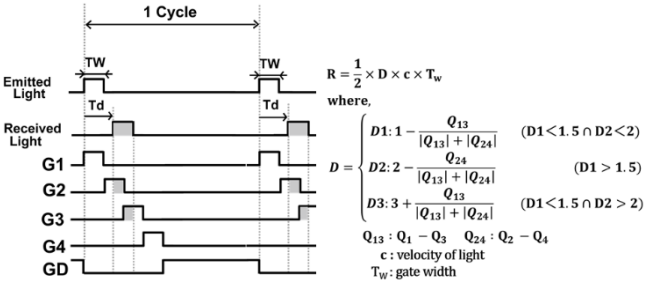

Fig3 Timing diagram for the lock-in pixel operation

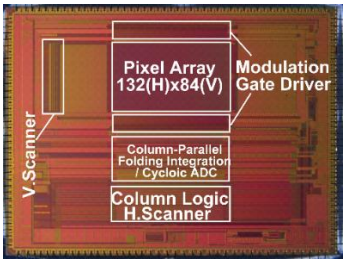

Fig.4 Chip micrograph

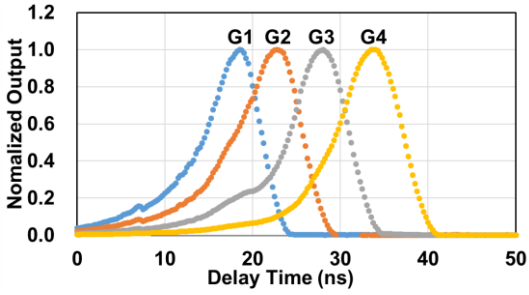

Fig.5 Modulation characteristic at 4ns light pulse and 850nm laser.

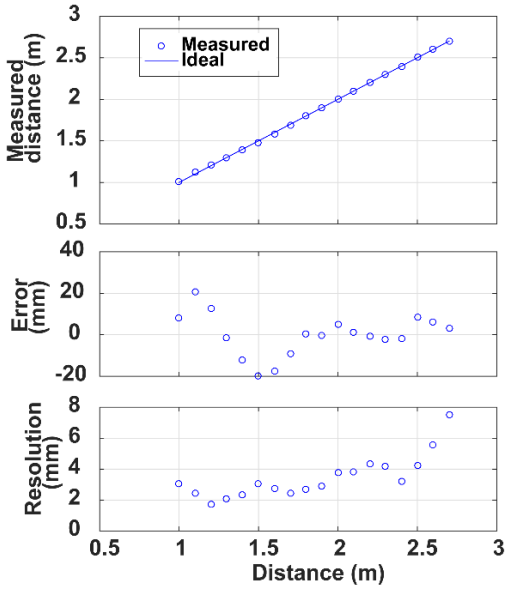

Fig. 6 Measured distance, error, and range resolution