Evaluation of Negative Capacitance Ferroelectric Field-Effect Transistors For Low Power Circuit Applications

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Abstract - Both digital and analog circuit performance of negative capacitance ferroelectric field-effect transistor (NC-FET) is evaluated based on its equivalent circuit model. $HfZrO_2$ is used as the ferroelectric with a reported damping constant ξ_{FE} of 10 Ω·m. Due to internal voltage amplification, both supply voltage V_{DD} and subthreshold swing of NC-FET are reduced as compared with the control. This could enable the employment of NC-FET in low-power and high-frequency digital circuits if ξ_{FE} is less than 10^{-2} Ω·m. In addition, NC-FET has I_{DS}-V_{DS} characteristic with a smaller output resistance at linear region and a larger resistance at saturation region, as compared with MOSFET. Therefore, NC-FET is beneficial in analog design such as lower on resistance in analog switch and more precise current transfer in the current mirror.

1. Introduction

Negative capacitance ferroelectric field-effect transistor (NC-FET) is a potential low power device with sub-60 mV/decade subthreshold swing (SS) [Fig. 1(a)] [1-15]. Most of the previous results confirmed the reduction of its supply voltage V_{DD} and subthreshold swing (SS) to suppress the rapidly increasing power density in digital circuits. However, its analog circuit performance is seldom discussed. In this work, a comprehensive evaluation on both digital and analog performance of NC-FET is provided.

2. Simulation Method

The dimensions of n- and p-channel devices (W_G/L_G) are 50 nm/50 nm and 100 nm/50 nm, respectively. 45 nm metal gate/high-k CMOS is used as the bottom structure and its electrical characteristics are predicted by BSIM4 in HSPICE. $HfZrO_2$ is used as the ferroelectric with Landau parameters α_{FE} = -8.5×10^8 m/F and β_{FE} = 1.8×10^9 m^5/F/C^2 and damping constant ξ_{FE} = 10 Ω·m. According to Landau-Khalatnikov equation (1), its equivalent circuit model is a series connection of a voltage controlled voltage source (VCVS) $V_{FE,S}$ and a resistor R_{FE} [Fig. 1(b)] [16, 17]. Here, t_{FE} is the ferroelectric thickness and V_{FE} is the voltage drop across it.

$$\xi_{FE}t_{FE}\frac{dP}{dt}+2\alpha_{FE}t_{FE}P+4\beta_{FE}t_{FE}P^3=V_{FE}. \quad (1)$$

3. Results and Discussion

Due to internal voltage amplification, a steeper swing in NC-FET is achieved [Fig. 2(a)]. Both V_{DD} (for I_{on} = 1.4 mA/μm) and threshold voltage V_T (I_T = 10 μA/μm) are reduced [Fig. 2(b)]. SS can be lower than 60 mV/decade when t_{FE} is larger than 20 nm [Fig. 2(c)].

For its output characteristics, a negative differential resistance (NDR) is observed when V_{GS} is 0.2 V [Fig. 3(a)]. This is attributed to Q_G modulation by V_{DS}. For V_{GS} = 0.5 V and 0.8 V, the output resistance R_{OUT} of NC-FET is smaller at linear region and larger at saturation region [Figs. 3(b) and 3(c)]. This feature is beneficial for analog design.

A three-stage inverter chain is used for circuit-level evaluation [Fig. 4(a)]. For a fair comparison with the same on/off-state currents, V_{DD} is set at 1.0 V and 0.71 V for MOSFET and NC-FET inverter chain, respectively. When ξ_{FE} is 10 Ω·m, the average propagation delay is 2.83 ns [Fig. 4(b)]. The dependence of delay on ξ_{FE} in Fig. 4(c) clearly shows that ξ_{FE} should be lower than 10^{-2} Ω·m for high frequency use.

Power evaluation in Fig. 5(a) demonstrates that, for ξ_{FE} = 10 Ω·m, short circuit power is dominant since an identical current flows through both NC-FETs. However, if ξ_{FE} can be lower than 10^{-2} Ω·m, either NC-FET is switched off so that short circuit power is eliminated and switching power consumes most energy [Fig. 5(b)]. Dependence of energy consumption on ξ_{FE} in Fig. 5(c) shows that NC-FET could be a lower power device than MOSFET for $\xi_{FE} < 10^{-2}$ Ω·m.

The lower R_{OUT} of NC-FET at linear region can be used in analog switch to provide smaller on-state resistance (Fig. 6). While the larger R_{OUT} at saturation region can be used in current mirror for more precise current transfer (Fig. 7).

4. Conclusions

NC-FET could achieve steeper swing than MOSFET. $\xi_{FE} \leq 10^{-2}$ Ω·m is required for the NC-FET to be used in low-power high-frequency digital circuits. The small R_{OUT} at linear region and larger R_{OUT} at saturation region could enable potential applications of NC-FET in analog circuits.

Acknowledgements

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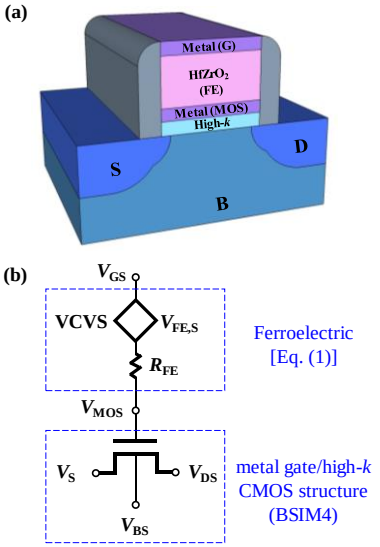

Fig. 1. (a) NC-FET structure. (b) Equivalent circuit model of ferroelectric (FE) consists of VCVS and R_{FE}.

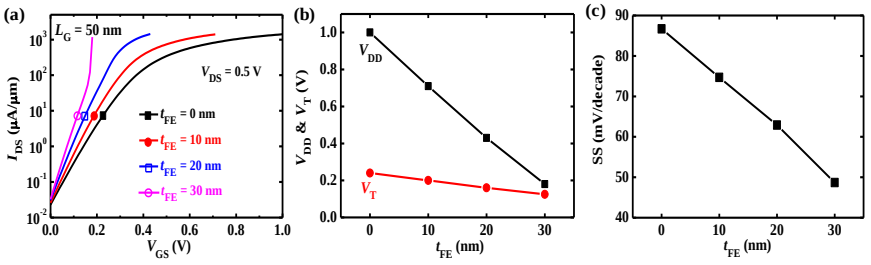

Fig. 2. (a) Steeper I_{DS}-V_{GS} characteristics of NC-FET with larger t_{FE}. (b) V_{DD} and V_T reduction with larger t_{FE}. (c) SS can be reduced to 48 mV/decade if t_{FE} is 30 nm.

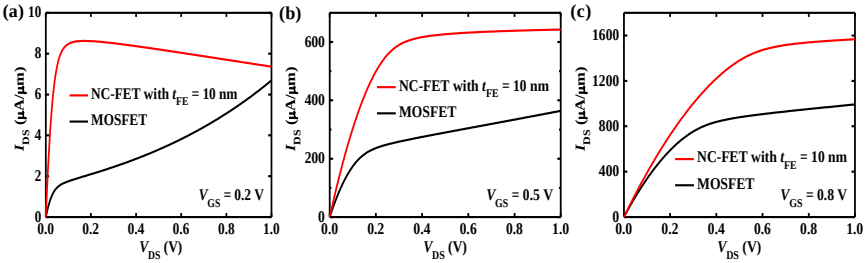

Fig. 3. Comparison of I_{DS}-V_{DS} characteristics between NC-FET (red) and MOSFET (black) at (a) V_{GS} = 0.2 V, (b) 0.5 V, and (c) 0.8 V. NDR is observed when V_{GS} is 0.2 V.

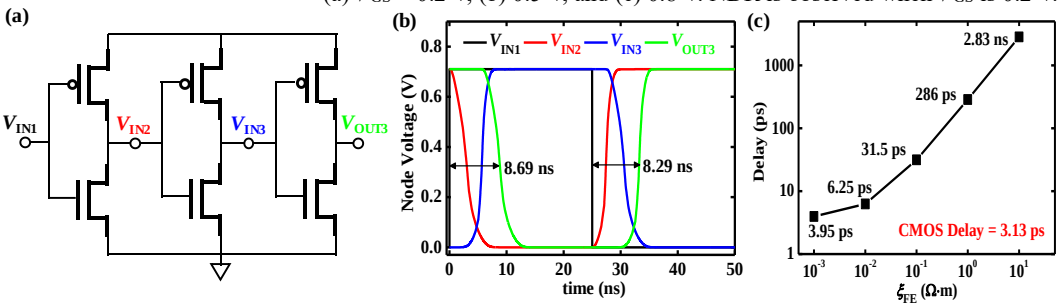

Fig. 4. (a) A three-stage inverter chain is used for digital evaluation. (b) Propagation characteristic shows that the average delay of each stage is 2.83 ns. (c) Dependence of delay on ξ_{FE} shows that $\xi_{FE} < 10^{-2}$ Ω·m is required to achieve the similar delay to MOSFET.

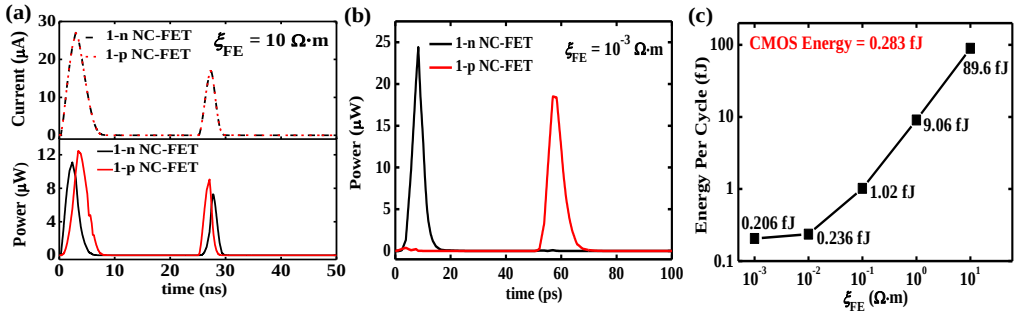

Fig.5. (a) The simultaneous power consumption of NC-FETs in the 1st stage indicates that short circuit power is dominant for ξ_{FE} = 10 Ω·m. (b) For $\xi_{FE} = 10^{-3}$ Ω·m, either NC-FET consumes energy during switching indicates that the dominant power is switching power $C_L V_{DD}^2$. (c) Dependence of energy consumption per cycle on ξ_{FE} shows that $\xi_{FE} \leq 10^{-2}$ Ω·m is required for low power circuit applications.

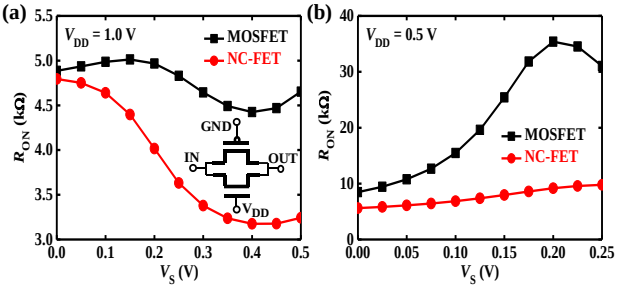

Fig. 6. Analog switch consisting of NC-FETs exhibits lower on resistance R_{ON} for both V_{DD} = 1.0 V in (a) and 0.5 V in (b).

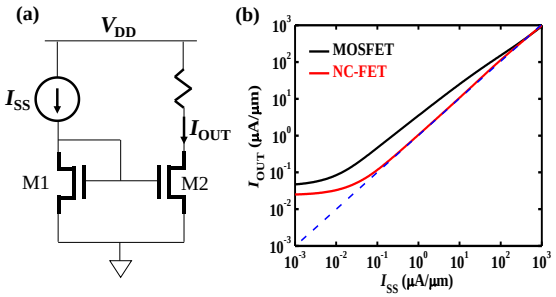

Fig. 7. Current mirror comprised by NC-FETs can transfer I_{SS} to I_{OUT} more precisely for a wide range.