K-5-02

Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp651-652

Time Domain Reflectometry of Organic Thin Film Transistor

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Abstract

We propose that time domain reflectometry is an novel and effective tool to investigate time behavior of the electronic devices. The carrier injection from the contact electrode into the organic thin film transistor is observed in 10 ns time resolution in our present experimental setup. Both vertical carrier injection into the thickness direction and horizontal diffusion at the semiconductor/insulator interface are observed with this method.

1. Introduction

Carrier injection from a contact electrode into a semiconductor attracts much interest all over the world. Many effective methods, for example TR-EFISHG[1] and charge modulation imaging etc., were proposed. However, the main target of these observation method was horizontal carrier diffusion at the semiconductor/gate insulator interface. Initial process of carrier injection from the contact electrodes into the semiconductor is vertically proceed into the thickness direction, and is not visible with these methods. Our research group has searched for novel method to observe both vertical and horizontal carrier injection.

In this work, we propose novel method for probing carrier injection process by using time domain reflectometry(TDR). TDR is a kind of impedance detection method by a step voltage wave. We added one additional idea to the conventional TDR to detect transient impedance of the device after application of voltage.

2. Sample preparation and *C-V* characteristics

Top contact and bottom gate thin film transistor (TFT) structure of the sample was prepared on a glass substrate. Pentacene thin film was formed by standard vacuum evaporation of which substrate temperature was room temperature. Although thickness of the pentacene layer in the present sample is thicker than that used in standard TFT structure, this is appropriate for the novel and basic study of TDR. Finally TFT structure was passivated by parylene-SR layer to reduce the effect of atmosphere. The sample was connected to pulse generator and sampler through transmission line. Figure 1 (b) is *C-V* characteristics of the pentacene TFT structure with a quasi-static *C-V* measurement. Capacitance of the sample increase with increasing negative bias voltage because of the carrier injection from the contact electrode into the organic semiconductor.

3. Principle of TDR measurement and equivalent circuit of TFT structure

TDR is one of the measurement to observe the discontinuity of the electrical impedance by using reflection or transmission of step voltage wave through the sample. We usually learn about impedance matching in a textbook of electrical measurement. If the transmission line of which characteristic impedance is 50 Ω has a discontinuity of the electrical impedance at the sample inserted in the transmission line, high frequency component of the voltage wave reflects at the impedance discontinuity, and the reflected waveform includes the electrical impedance of the sample. The advantage of this method is to acquire the transient electrical impedance, not steady state.

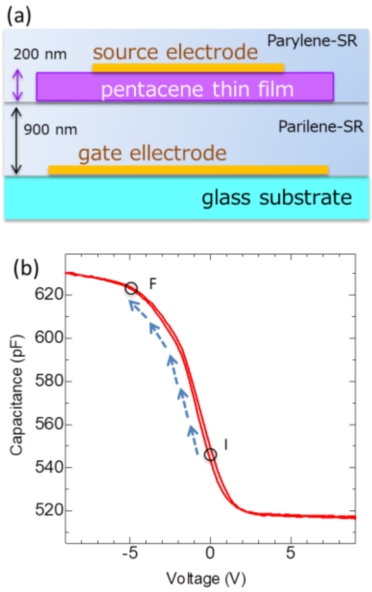

Figure 1 (a) Top contact and bottom gate configuration of pentacene thin film transistor structure, and (b) *C-V* characteristics of the sample.

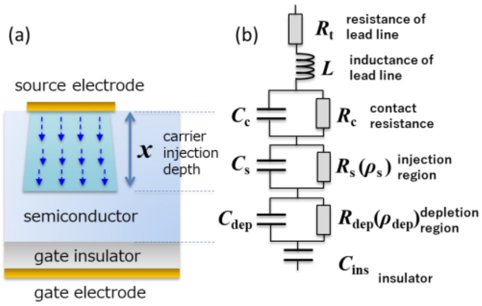

Figure 2 (a) schematic illustration of the carrier injection. and (b) equivalent circuit of the TFT structure during carrier injection.

Our idea to observe the transient electrical impedance is very simple. We applied rectangular pulse wave to the sample although the step wave is usually used in conventional TDR. In the observed TDR wave, rise edge include the initial impedance of the sample if the pulse interval is sufficiently long, and fall edge include the transient impedance after application of the voltage during pulse width. Time domain transmission (TDT) also include the sample impedance, we chose to observe TDT signal.

Figure 2 (a) and (b) shows the schematic illustration of transient carrier injected state of the sample and the corresponding equivalent circuit, respectively. Depth from the contact electrode edge to the frontline of the injected carrier distribution was defined as *x*. The semiconductor layer was divided into two layer, the corresponding carrier injected region and depletion region, so these two region were expressed as a pair of series connection of parallel *C* and *R*. In addition, parasitic inductance and resistance of lead line are also considered.

4. Results and discussion

Figure 3 shows the observed time domain transmission (TDT) signal with various pulse width, and the dashed lines are calculated fitting curves. The baseline of the applied voltage wave was 0 V and the pulse height was -5 V. In this condition, electrical impedance of the sample varies from initial value (point I in Fig.1(b)) to final value (point F) after the sufficient voltage application time. As shown in the figure, each fitting curves well express the experimental TDT voltage waveforms. Main variable parameters in calculating the fitting curve to express the pulse width variation were carrier injection depth *x*, resistivity of carrier injected region ρ_s, and capacitance of gate insulator C_{ins}. *x* increases with the progress of the vertical carrier injection toward the thickness direction. ρ_s decreases with increasing injected carrier density. C_{ins} increase with the in-plane expansion of the carrier distribution at the semiconductor/gate insulator interface.

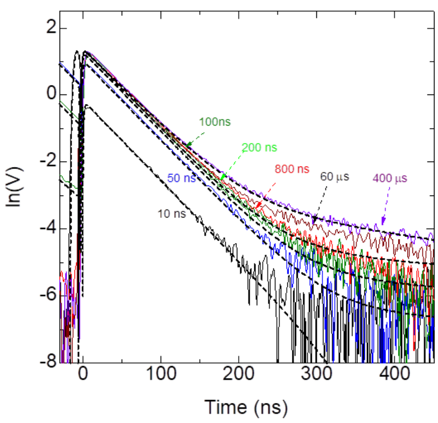

Figure 3 Observed TDT waveform in the fall edge region. Dashed curves are fitting curve.

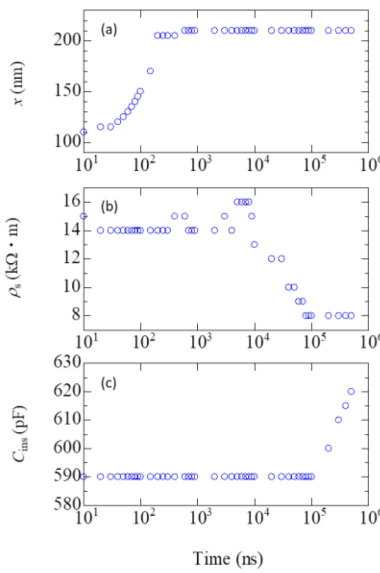

Figure 4 Time variation of the three main parameters of *x*, ρ_s, C_{ins}.

Figure 4 is summary of the three fitting parameters. In the early stage of the carrier injection, *x* increase from the natural penetration depth of approximately 100 nm toward the thickness of the semiconductor layer within 200 ns. After that, ρ_s begin to decrease with the accumulation of the hole. C_{ins} finally begin to increase with the spreading of the in-plane hole distribution at the channel region. The observed long delay of increase of C_{ins} is possibly explained by highly distributed carrier trap site at the semiconductor/insulator interface. The result of the time dependent hole distribution calculated with the device simulator (AdvanceSoft Corporation) support the experimental results.

5. Conclusions

In this work, we presented that TDR can track the carrier injection process by observing transient electrical impedance of the organic TFT structure.

Acknowledgements

We would like to acknowledge AdvanceSoft Corporation for giving us an opportunity to try ADVANCE/TCAD device simulator. Calculated results of the device simulation were helpful for us to understand the carrier injection. Part of this work was financially supported by JSPS KAKENHI Grant Number 17H02761.

References

[1] T. Manaka et al., Nature Photonics **1** (2007) 581.