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Logic Circuits Consisting of Pentacene Thin-Film Transistors with Controlled Threshold Voltages

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Abstract

Pentacene thin-film transistors (TFTs) with controlled threshold voltages have been used for logic circuits. The threshold voltage control was demonstrated by oxygen plasma treatment to the surface of the SiO_2 gate dielectric. Ring oscillators consisting of the enhancement/depletion inverters successfully operated at voltages of 14 to 20 V.

1. Introduction

Organic thin-film transistors (TFTs) have attracted much attention because of their potential for applications such as logic circuits and flat panel displays [1-3]. Threshold voltage control is a critical issue for such applications of organic TFTs. Some groups have attempted threshold voltage control for organic TFTs using several approaches [4-8].

We have carried out to control the threshold voltage in organic TFTs having SiO_2 gate dielectrics using oxygen plasma treatment to the gate dielectrics [9-11]. The advantage of the fabrication process is that it does not require additional structures such as second gate electrodes and self-assembled monolayers with dipole moments. The threshold voltages can be controlled by changing the treatment time. We can fabricated enhancement- and depletion-type pentacene TFTs by two-step surface treatment, and applied the TFTs for the construction of logic inverter circuits. The inverters successfully operated under measurement condition for static characteristics [11]. However, the investigation of the dynamic characteristics is demanded for actual applications.

In this study, we fabricated ring oscillators consisting of enhancement/depletion (E/D) inverters and investigated the dynamic characteristics. The two-step surface treatment for the gate dielectrics was applied for fabrication of the enhancement- and depletion-type pentacene TFTs.

2. Experimental

Figure 1(a) shows cross-section of a fabricated inverter. The enhancement- and depletion-type pentacene TFTs were used for the PMOS1 and PMOS2 in the circuit shown in Fig. 1(b), respectively. The Au/Cr layer on the glass substrate serves as wiring between transistors.

Figure 2 shows the fabrication process for the ring oscillator. The pentacene TFTs were fabricated on a glass substrate flattened by a polymer layer. The flattening process contributes to improvement of the field-effect mobility in TFTs. The SiO_2 gate dielectric had a thickness of 130 nm and a unit area capacitance of 31 nF/cm^2. The surface of the gate dielectric for PMOS2 was exposed to oxygen plasma for 180 s. Then, the whole area was treated with the UV/ozone. After the treatment, the substrate was immediately exposed to hexamethyldisilazane (HMDS) vapor to obtain a hydrophobic surface. The 45-nm-thick pentacene was deposited through a shadow mask to form channel region. Then, the fabrication of circuit was completed by deposition of Au for drain/source electrodes. The channel width and length were 600 mm and 40 mm, respectively. The characteristics were measured in a dry-nitrogen-filled glovebox.

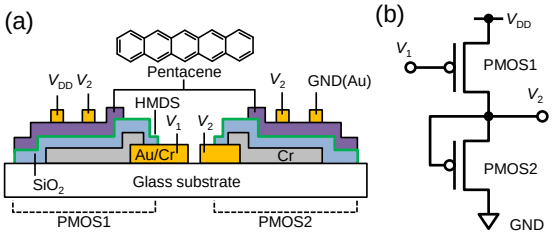

Fig. 1 (a) Cross-section and (b) circuit of a fabricated inverter consisting of enhancement- and depletion-type pentacene TFTs.

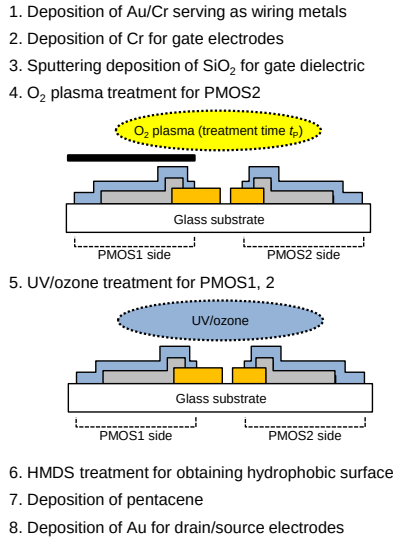

Fig. 2 Fabrication process of pentacene TFTs in ring oscillators.

3. Results

Figure 3(a) shows the drain current (I_D) versus gate voltage (V_G) characteristics of pentacene TFTs for PMOS1 and PMOS2. The characteristics exhibit no large hysteresis in the forward and reverse sweep. The threshold voltages of

the TFTs for PMOS1 and PMOS2 were -2.5 V and 8.8 V, respectively. The values are close to design values. Figure 3(b) shows the input/output characteristics of an E/D inverter at V_{DD} voltages of 5, 10, 15, and 20 V. The circuit operated as an inverter at voltage in the range of 10 and 20 V. The switching voltages at V_{DD} = 10, 15, and 20 V are 1.8, 6.4, and 11.3 V, respectively. The values are consistent with those calculated from the threshold voltages and field-effect mobilities. Although the switching voltage at V_{DD} = 10 V was obtained, the low noise margin was not defined.

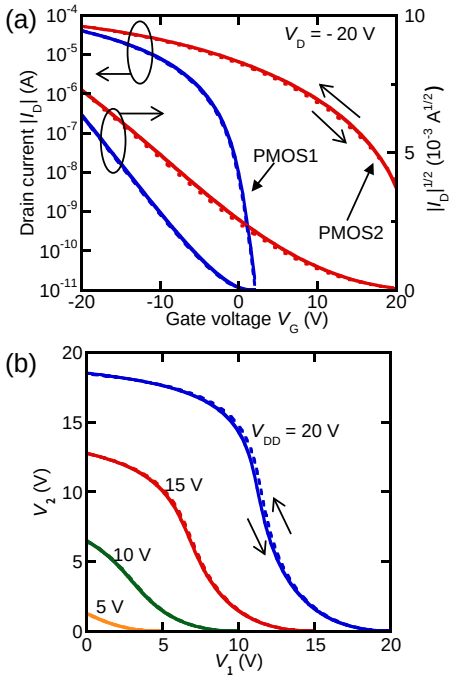

Fig. 3 (a) Transfer characteristics of pentacene TFTs for PMOS1 and PMOS2. (b) Input/output characteristics of an E/D inverter measured at V_{DD} = 5, 10, 15, and 20 V.

The photograph and the circuit of a fabricated five-stage ring oscillator with an output buffer are shown in Figs. 4(a) and 4(b), respectively. The output oscillation was observed at V_{DD} = 14 V or higher voltages. Minimum supply voltages for oscillation relate to noise margin estimated from input/output static characteristics. Since the inverter has no noise margin at V_{DD} = 10 V, no operation at less than 14 V is consistent with the static characteristics.

Figure 4(c) shows the waveform of output characteristics at V_{DD} = 20 V. The waveform was measured using a digital oscilloscope with an active probe. The oscillation frequency (f) at V_{DD} = 20 V is about 256 Hz. The intrinsic signal delay per stage (t_i) is calculated to be 0.33 ms using t_i = $1/[2(N+1)f]$ where N is the number of inverters in the circuit [12]. To support the operation frequency, we simulate the output characteristics of a ring oscillator with SPCIE circuit simulator assuming the practical parameters including field-effect mobilities, threshold voltages, and parasitic capacitance. As a result, we obtained a similar waveform and an oscillation frequency close to the experimental value.

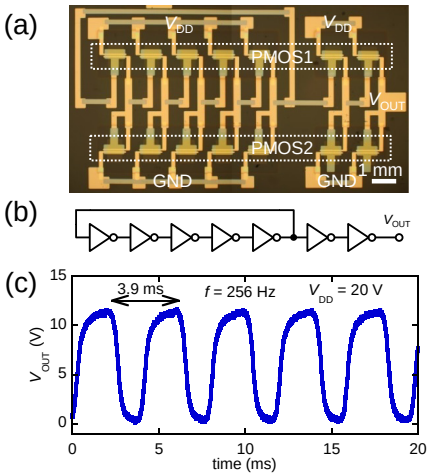

Fig. 4 (a) Photograph and (b) circuit of a five-stage ring oscillator with an output buffer. (c) Output characteristics of a ring oscillator at a voltage of 20 V.

4. Conclusions

In conclusion, ring oscillators consisting of pentacene TFTs with controlled threshold voltage successfully operated. The oscillation frequency was consistent with the static characteristics of the TFTs. The result supports that the threshold voltage control is useful for circuits operating dynamically.

Acknowledgements

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