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High-performance and low-power 2D transition-metal dichalcogenide field-effect transistors

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Abstract

Two-dimensional transition-metal dichalcogenides (TMDs) represent a promising class of materials for electronic and photonic devices, benefiting from their high mobility, tunable bandgap and ultrathin body. In this context, we carry out systematic investigations on high performance and low power TMDs field-effect transistors (FETs). We observed large density of atomic defects in monolayer MoS_2 lattice, resulting in hopping transport of MoS_2 transistors, and a facile thiol chemistry can repair the sulfur vacancies and improve the interface quality, leading to significant reduction of impurities and traps. In combination with high-κ dielectrics, we achieve record-high room-temperature mobility of ~150 cm^2/Vs and 83cm^2/Vs for monolayer MoS_2 and WS_2, respectively. We further develop a theoretical model to quantitatively correlate these scattering sources to measured electrical data. For low power application, we realize steep-slope MoS_2 n-type negative capacitance FETs (NCFETs) using ferroelectric (FE) $HfZrO_x$ (HZO)/AlO_x as dielectric. The MoS_2 NCFET devices exhibit ultra-low subthreshold swing (SS) of 23 mV/dec, sub-60mV/dec over 6 orders of I_D and nearly hysteresis-free. Our study paves the way for high-performance and low-power applications of TMDs.

1. Introduction

Microelectronic devices continue to develop along the Moore's Law for more than 50 years and are facing challenges such as limitation of physical scaling and high power consumption.[1] The 2D semiconductor, represented by TMDs, with atomic thickness and tunable bandgap show a promising material revolution in electronic and optoelectronics devices. However, the charge transport in monolayer of TMDs is dominated by many extrinsic factors and carrier mobility is still far away from the intrinsic limitation.[2]

Here, we report the mobility engineering in monolayer MoS_2 and WS_2 by combination of transport theory and experimental methods. Record-high room-temperature mobility of ~150cm^2/Vs7 and 83cm^2/Vs are achieved for monolayer MoS_2 and WS_2, respectively. Our combined experimental and theoretical study provides a clear path towards intrinsic charge transport in TMDs for future high-performance device applications.

Furthermore, we report the MoS_2 NCFETs using HZO as a dielectric layer, showing impressive device characteristics, including minimum SS of 23 mV/dec, sub-60 mV/dec operation for over 6 decades, negligible hysteresis. The 2D NCFETs demonstrate new low power application potential for future devices.

2. High Performance TMDs MOSFETs

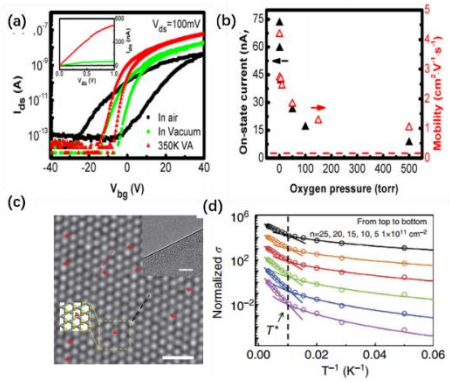


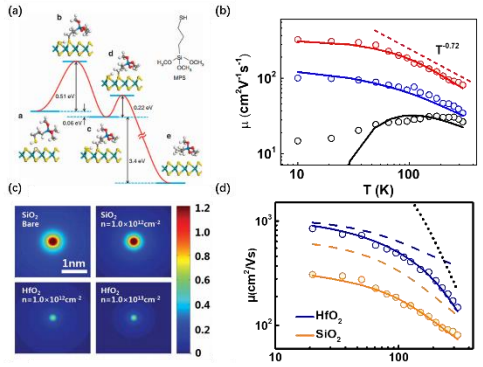
Figure 1. (a)I_d-V_g characteristics of MoS_2 FET in different ambient (b)On-state current and mobility versus O_2 pressure (c)HR-TEM of monolayer MoS_2 (d)Arrhenius plot of normalized conductivity and the fitting results by hopping model

We report that chemisorption of both oxygen and water from ambient causes degradation of conductance to ~100 times. After annealing *in-situ* at 350 K under high vacuum, the on-state current gradually increased to a stable level of ~5 times higher (Fig. 1a, b). [3]To reveal nature of the disorders, we performed HR-TEM characterizations. The HR-TEM shows a large number of sulfur vacancies on MoS_2 (Fig. 1c). Together with DFT calculation, we proposed a transport model in which low-carrier-density transport is dominated by hopping among defect-induced localized states(Fig. 1d).[4]

Next, we employed thiol chemistry to repair the sulfur vacancies(Fig. 2a), resulting in significant reduction of the charged impurities and traps. Record-high mobility greater than 80 cm^2/Vs is achieved in back-gated monolayer MoS_2 FET at room temperature(Fig 2b).[5] Furthermore, we perform a combined experimental and theoretical study of the charge transport in unprecedented phonon-limited mobility of ~150cm^2/Vs attained in our samples at room temperature, due

to suppression of Coulomb impurity scattering through dielectric and carrier screening.(Fig 2c-d)[6,7]

Figure 2. (a)Schematic of the reaction between SV and MPS (b) μ-T characteristics for the three MoS_2 devices with best theoretical fittings (c)Space distribution of Coulomb potential for a point charge in MoS_2 (d) μ-T characteristics for MoS_2 devices on SiO_2 and HfO_2 with best theoretical fittings



To understand the underlying limitations in current MoS_2 FETs, we review the scattering mechnisms and charge traps in MoS_2 from theoretical view, and establish our theoretical model with detailed parameters. Then, we use our model to analyze the available high performance monolayer MoS_2 FET data from literature.(Fig. 3) We shed light on the microscopic origin behind the low mobility in various MoS_2 FET structures.[2]

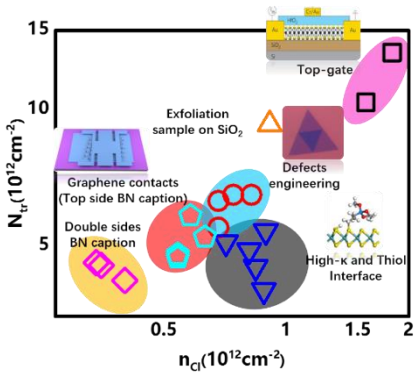
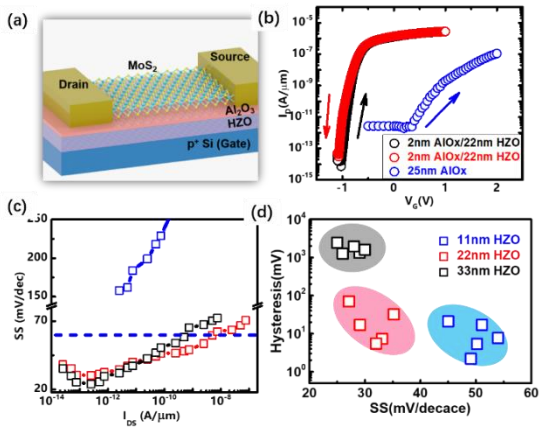


Figure 3. Traps and impurities distribution of MoS_2 devices with different processes

3. Low power MoS_2 NCFETs

We report the steep-slope MoS_2 n-type Negative Capacitance Field Effect Transistors (NCFETs) with minimum SS of 23mV/dec using different thickness ferroelectric(FE) $HfZrO_x$ (HZO)/AlO_x as dielectric. The subthreshold slope(SS) and hysteresis of MoS_2 NCFETs show obvious FE thickness dependence. As eclectic results, we find NCFETs on 22nm HZO remain a reduced SS of 23mV/dec without obvious hysteresis.(Fig. 4) Furthermore, we compare the on-current versus on/off ratio of reported and our NCFETs together at defined V_{DD}=0.5V. MoS_2 NCFETs on 22nm and 11nm HZO show large on/off ratio of over 10^7 with considerable current of over 2μA.[8]

Figure 4. (a)Schematic of MoS_2 NCFET (b)(c)Performance comparison between PCFET and NCFET (d)Thickness dependence of SS and hysteresis for MoS_2 NCFETs



4. Conclusions

We achieved record-high mobility greater than 150cm^2/Vs in back-gated monolayer MoS_2 FET at room temperature by defect and interface engineering. Then, we developed a theoretical model to systematically understand the mobility, conductivity, and metal-insulation transition in monolayer MoS_2. Moreover, we demonstrated MoS_2 NCFET with impressive device characteristics using $HfZrO_x$ as gate dielectric for low power applications.

Acknowledgements

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Appendix

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