Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp717-718

Interface traps "extrinsically" deliver MIT in monolayer MoS_2 FET

Nan Fang and Kosuke Nagashio
Department of Materials Engineering, The University of Tokyo
7-3-1 Hongo, Tokyo 113-8656, Japan
Phone: +81-3-5841-7161 E-mail: nan@adam.t.u-tokyo.ac.jp

Abstract

Field-effect control of carriers are systematically studied by both *I-V* and *C-V* in MoS_2 FET. MIT origin in 2D materials is investigated. It is suggested that C_{it}-enhanced positive V_{TH} shift artificially induces the "extrinsic" MIT.

1. Introduction

The electrostatic field-effect control of carriers determines most of the device characteristics and needs to be fully understood before exploring the underlying physics in the electrical transport properties, for example, metal-insulator-transition (MIT) in MoS_2 and other 2D materials [1-3]. As for monolayer MoS_2, the carrier modulation by the gate is mainly determined by the following two factors, in addition to the geometric capacitance (C_{ox}). Intrinsically, it is limited by the quantum capacitance (C_Q), which comes from low density of states (DOS) of MoS_2 and Fermi-Dirac distribution. Extrinsically, it is also severely affected by the interface trap capacitance ($C_{it} = e^2D_{it}$). Therefore, by intensively investigating the high-*k*/MoS_2 FET with *C-V* measurement so far, we have elucidated all the constituents of the total capacitance ($1/C_{total}=1/C_{ox}+1/(C_Q+C_{it})$) [4].

In this study, on the basis of well extracted C_Q and C_{it}, we first reproduce MIT in *I-V* characteristics by utilizing the drift current model. Then, through this modeling, we would like to indicate that the origin of MIT is external outcome resulting from C_{it}.

2. Experiments

Monolayer MoS_2 films are mechanically exfoliated on insulating quartz substrate from natural bulk MoS_2 flakes. Ni/Au was deposited as source/drain electrodes. Then, 1-nm Y metal was deposited via thermal evaporation of the Y metal in a PBN crucible at an Ar atmosphere with a partial pressure of 10^{-1} Pa, followed by oxidization at atmosphere to form buffer layer. 10-nm Al_2O_3 oxide layer was deposited by atomic layer deposition. The Raman measurement was employed for determining the layer number. The electrical measurements were performed in the vacuum prober. Alternatively, the back-gate four-probe FET with monolayer MoS_2 on 90-nm SiO_2/n^+-Si substrate is prepared for MIT study.

3. Quantum capacitance in monolayer MoS_2

Fig. 1 shows the schematic drawing and the optical image of top-gate monolayer MoS_2 FET on quartz substrate for *C-V* measurement. Quartz substrate was used to totally suppress parasitic capacitance. Films with large area (>30 μm^2) were selected for device fabrication and characterization. C_Q was originally derived from partially screening in 2D electron gas [5]. As for monolayer MoS_2, C_Q originates from partially occupied density of states (DOS) of

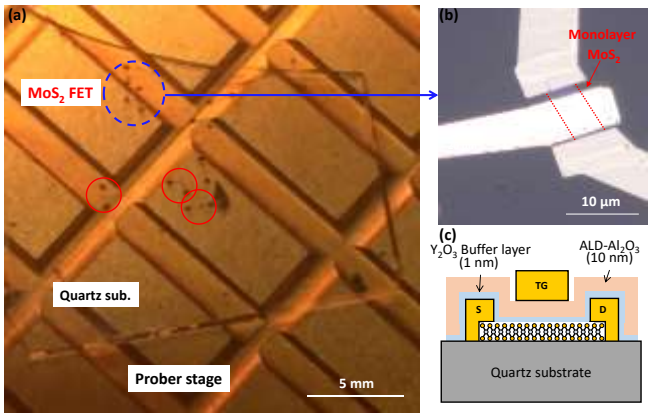

Fig. 1 (a,b) Optical image and (c) schematic diagram of top-gate monolayer MoS_2 FET.

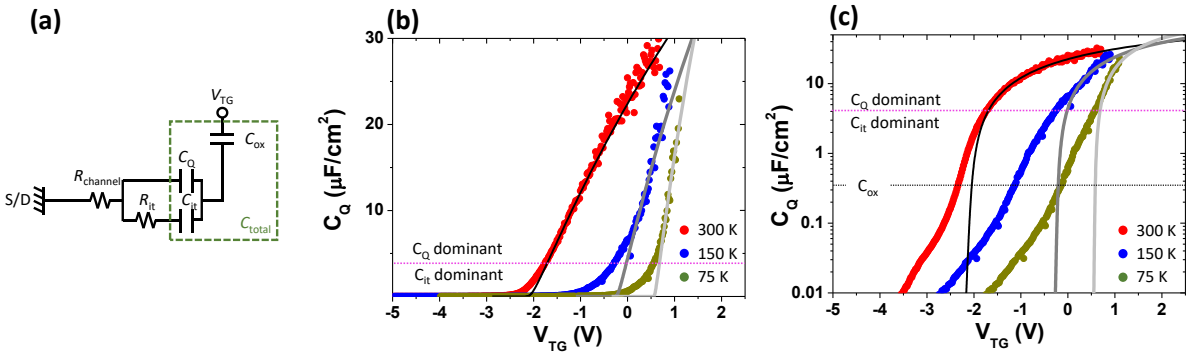

Fig. 2 (a) Equivalent circuit of C-V measurement in MoS_2 FET. (b) C_Q extracted as a function of V_{TG} at 300 K, 150 K and 75 K. Solid lines are the theoretical fitting curves. (c) The same figure as (b) with the logarithmic scale.

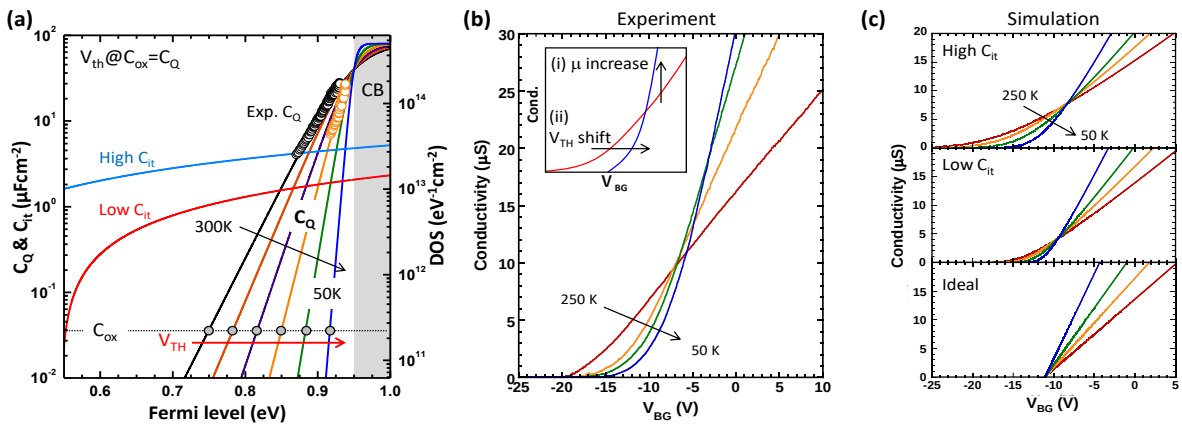

Fig. 3 (a) C_{it} and C_Q extracted and calculated at different temperatures (300 & 150 K for exp.). High and low C_{it} lines are used for the simulation. (b) Experimental 4P conductivity as a function of V_{BG} at 50~250 K. (c) Simulated σ-V_{BG} curves with different C_{it} levels.

CB modulated by Fermi energy (E_F) in Fermi-Dirac distribution. Here, C_Q is experimentally extracted from capacitance between source/drain and top-gate. The simplified circuit is shown in **Fig. 2a**. By neglecting the access resistance effect at accumulation region and extracting C_{ox}, C_Q and C_{it} can be extracted. **Fig. 2b, c** shows experimentally extracted C_Q from *C-V* at 1 MHz for temperature range of 75~300 K. The extracted C_Q-V_{TG} curves are divided into two regions. The first region is the C_Q dominant region, with $C_Q > C_{it}$. In this region, C_Q has a clear temperature dependence and fits well with the theoretical calculation. The slope of C_Q becomes sharp at low temperatures due to the intrinsic nature of the Fermi distribution, which provides an alternative means to confirm the validity of C_Q extraction. The other region is the C_{it} dominant region, with $C_Q < C_{it}$. The C_Q-V_{TG} curve deviates from theoretical curve and shows a gradual change with decreasing temperature.

4. MIT origin in monolayer MoS_2

Having confirmed C_Q, carrier density in the CB can be directly estimated. Drift current model is then used to simulate carriers transport process, which enables us to correlate *I-V* with *C-V*. C_{it} degrades the field-effect control of carriers through following equation.

$$V_{T/BG} = V_{T/BG,mid-gap} + \int_0^{E_F/e} (C_Q + C_{it} + C_{ox}) / C_{ox} d(E_F / e) \quad (1)$$

MIT is often observed in 2D materials as cross-over point in *I-V* for different temperatures. This *I-V* curve is reproduced by above simulation. **Fig. 3a** shows C_Q and C_{it} in the monolayer MoS_2 FETs for different temperatures. **Fig. 3b** shows experimental conductivity (σ)-V_{BG} characteristics from four-probe back-gate device, which clearly shows MIT. Experimental σ-V_{BG} characteristics is simulated with three different C_{it} levels (high, low and no C_{it}) and plotted in **Fig. 3c**.

MIT can be observed intuitively by the combination of (i) the increase in the mobility and (ii) positive V_{TH} shift with decreasing the temperature. Within the present model, the mobility is assumed to increase with decreasing temperature due to suppression of phonon scattering. Therefore, the dominant key factor for MIT is a positive V_{TH} shift with decreasing temperature. This occurs because E_F at V_{TH} approaches the conduction band edge at lower temperature since V_{TH} is defined by V_{BG} at $C_Q = C_{ox}$, which is shown in **Fig. 3a**. Thus, a larger amount of C_{it} needs to be filled by electrons before reaching V_{TH} at lower temperature, resulting in the V_{TH} shift. By decreasing the C_{it} level, the crossover points of the MIT (shown by arrow in **Fig. 3c**) get close to V_{TH} and finally enter the subthreshold region for the case with no C_{it}, which is the ideal V_{TH} shift.

Recently, no MIT has been reported for an *h*-BN-encapsulated monolayer CVD-MoS_2 FET, suggesting a quite low C_{it} due to superior 2D/2D interface properties [6]. It should be noted that ultra-thin 2D materials with reduced DOS is more sensitive to the interface disorder, since the carrier modulation is controlled by the relative magnitude of C_Q and C_{it}. The present model indicates that C_{it}-enhanced positive V_{TH} shift is one of the main origins for "extrinsic" MIT. Cross-over point in *I-V* is just the outcome of carrier band transport under degraded field-effect modulation for different temperatures.

5. Conclusions

Field-effect control of carriers were systematically studied by both *I-V* and *C-V* in monolayer MoS_2 FET. C_{it}-enhanced positive V_{TH} shift is suggested to be one of the main origins for "extrinsic" MIT.

Acknowledgements
NF was financially supported by JSPS KAKENHI. This research was partly supported by the JSPS Core-to-Core Program, A. Advanced Research Networks, JSPS KAKENHI Grant Numbers JP16H04343, Japan.

References

[1] B. Radisavljevic *et al.*, Nature Materials 2013, **12**, 815. [2] X. Chen X *et al.*, Nature Commun. 2015, **6**, 6088. [3] Z. Yu *et al.*, Nature Commun. 2014, **5**, 5290 [4] N. Fang *et al.*, J. Phys. D 2018, **51**, 065110. [5] S. Luryi, Appl. Phys. Lett.1988, **52,** 501. [6] X. Cui *et al.*, Nature Nanotech. 2015, **10**, 534.