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V_{th} control in p-type graphene barristor using a polymer doping process

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Abstract

P-type graphene barristors are fabricated using graphene- Dinaphtho- [2,3-b: 20,30f] thieno [3,2-b] thiophene(DNTT) Schottky junction with a polymer layer controlling the threshold voltage. Using complimentary barristors doped with PEI and PAA polymers, inverters with gain values in the range of 0.7-2.5 have been demonstrated.

1. Introduction

Graphene barristor, that takes advantage of the Schottky barrier formed along the channel at the interface graphene-semiconductor, has emerged as promising device for logic circuits because it shows high on/off ratio [1]. Graphene barristor operates by modulating the graphene/semiconductor Schottky barrier since the Fermi level of graphene can be controlled by external field. Various researches have demonstrated *n* and *p* type barristors using respectively *n* and *p* type semiconductors. However, barristors present a challenge because their threshold voltage (V_{TH}) is not easily controllable due to the absence of body contact. Controllable V_{TH} is absolutely necessary for barristors application in logic circuits. Several approaches, such as stacking Al_2O_3/SAM bilayers or e-beam treatment, have been proposed to control V_{TH} in triode devices [2,3]. The so-called charge injection layer (CIL) approach consists of arranging a polymer between graphene and semiconductor in order to create a charge injection layer [4,5,6]. Since we are focusing here on p-type barristor, DNTT was used as a p-type semiconductor because it shows good stability in ambient conditions [7]. By forming a CIL at the interface graphene/DNTT, we successfully controlled SBH and V_{TH}. In fact, electrical measurements showed SBH-tuning when the CIL was disposed between graphene and DNTT.

Using barristor with different V_{TH} we demonstrated inverters with promising gain values.

2. Experiment

In order to fabricate the p-type barristor, Ti(20nm)/Au (50nm) gate-metal were deposited on bare substrate using e-beam evaporator. The device was then washed in SC1 before the deposition, using ALD, of a 20nm aluminum oxide layer. Vacuum annealing was then performed and CVD-graphene transferred on the insulating film via a wet transfer following PMMA method. After graphene transfer, a 30 nm gold was deposited and served as hard mask to pattern the channel by etching the useless graphene in O_2 plasma. Au hard mask was then removed in a wet etching process. Thereafter, graphene channel was covered with 0.2 wt% Poly-ethylenimine (PEI) and 2 wt% Poly-acrylic acid (PAA) solution during 3hours. The device was rinsed in ethanol during 10 seconds. 150nm of DNTT was deposited through a shadow mask, at the rate of 0.2Å/s, by thermal evaporation, Fig. 1. 100nm S/D electrodes were finally deposited by e-beam evaporator, Fig. 1. All devices, namely GFET, DNTT TFT and barristors, were fabricated at the same time.

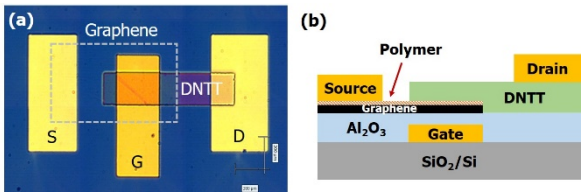

Fig. 1 Optical image (a) and schematic cross section (b) of the fabricated graphene-DNTT barrister.

Electrical characteristics of all devices were recorded using a Keithley 4200 parameter analyzer.

2. Results and discussion

The equilibrium band diagrams of graphene-DNTT based barristor with different polymers are shown in Fig. 2(a). Since PEI is nucleophile it will react by increasing the Fermi level of graphene and lowering the doping concentration in DNTT. Thereby, the width of the depletion layer in DNTT is increased leading to larger SBH. On the other hand, PAA is electrophile so it will lower the Fermi level of graphene and increase the doping concentration of DNTT. This will result

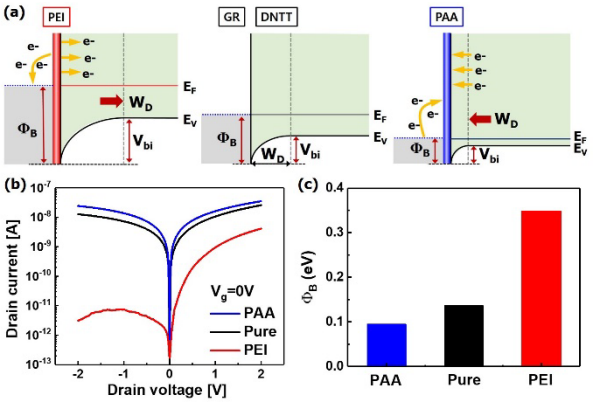

Fig. 2 (a) Band diagram structure of graphene-DNTT barristors (b) I_dV_d characteristics. (c) Extracted SBH values of the graphene-DNTT barristors.

in reducing the depletion in DNTT.

The output characteristics of Graphene-DNTT barristors are shown in Fig. 2(b). The saturation current, at V_d= -2V, is about ~10^{-11}, ~10^{-8} and ~2x10^{-8}Amps, respectively for, PEI-coated, CIL-less and PEI-coated barristors.

The SBH values were extracted from temperature dependence of drain current and are shown in Fig. 2(c). Graphene-DNTT barristor coated with PEI presents the highest SBH, 0.35eV. The undoped and PAA-doped barristors present respectively SBH of 0.14 eV and 0.08 eV.

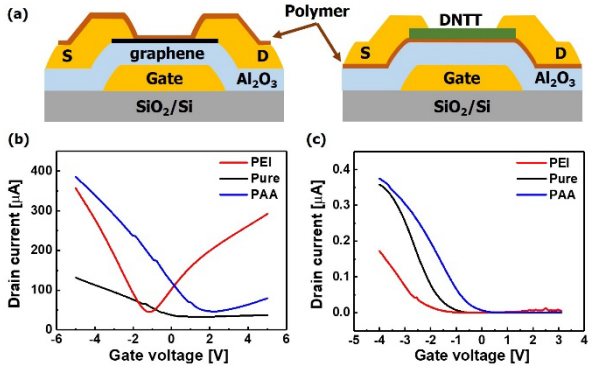

Fig. 3 (a) Scheme view of GFET and DNTT TFT with a polymer. Transfer characteristics of (b) GFET and (c) DNTT TFT devices.

As mentioned above, when a polymer is inserted between graphene and DNTT in p-type barristor, the SBH varies depending on the polymer properties. To illustrate the effect of polymers on graphene and DNTT, GFET and DNTT-TFT witness samples were fabricated. They were then doped by the same polymers used above in order to apprehend their effect on the electrical response, Fig. 3(a). Notice that the polymer is disposed above the graphene-layer in the GFET and under the DNTT-layer in the DNTT TFT.

Fig. 3 shows that the Dirac voltage of graphene shifts to lower (higher) values in the case of PEI (PAA). This signify that the Fermi level of PEI (PAA) doped graphene in GFET is lower (higher) compared to that of graphene in the bare GFET. Similarly, in the case of DNTT TFT, Fig. 3(c), V_{TH} shifts to the left (right) in PEI (PAA) DNTT-TFT indicating lower (higher) carrier concentration of DNTT. This can be explained by the fact that PEI (PAA) promotes (suppresses) electron transport in the DNTT.

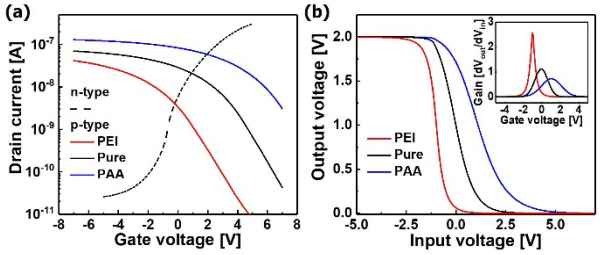

Fig. 4 (a) Transfer characteristics of n-type, polymer-coated p-type barristor (b) Inverter characteristics and the corresponding gain values.

Finally, the electrical results obtained above on the graphene-DNTT barristors were used in a simulation that aims to demonstrate inversion properties. Indeed, inverter characteristics were clearly demonstrated as shown in Fig. 4. The output voltage was found too high in case of low input voltage, and vice-versa, Fig. 4(b). The gain values of the PEI, PAA doped and undoped inverters are respectively ~ 2.5, ~ 1.1 and 0.7. These results show that PEI allow the best result (most steeper inverter) and the highest gain, in comparison to the undoped and the PAA-doped counterparts.

3. Conclusion

Two different polymers were successfully inserted in complex channel composed of graphene and DNTT. This allowed to tune the Fermi level of graphene and hence to control the carrier concentration of DNTT in a p-type barristor. The SBH was controlled and resulted in predicted V_{TH} shift. The PEI-coated *p*-type barristor fabricated in this work showed better inverter characteristics and seems very practical for logic circuits.

Acknowledgements

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