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Study on origin for D_{it} through SS in monolayer MoS_2/*h*-BN/graphite FET

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Abstract

Subthreshold swing (SS) for monolayer MoS_2/*h*-BN/graphite heterostructure FET was studied to reveal the origin for the interface states density (D_{it}). SS was estimated as ~80 mV/dec at room temperature and showed the clear temperature dependence. Based on the comparison of SS for different device structures, the origin for D_{it} is suggested to be the strain introduced in MoS_2 during the top gate high-*k* deposition.

1. Introduction

The understanding of the interface properties in high-*k*/MoS_2 system is crucial in ultimate scaled device research. The interface states density (D_{it}) at the high-k/monolayer MoS_2 interface has been reported to exhibit the band tail energy distribution [1], which is suggested to be resulted from the bond bending of Mo *d* orbital since the conduction and valence band of MoS_2 consist of the energy splitting of Mo *d* orbital in the ligand field of S. Therefore, two possible origins are expected; one is the strain introduced due to the deposition of top-gate insulator, the other is the roughness of SiO_2 substrate.

In this study, monolayer MoS_2 was placed on the atomically flat surface of *h*-BN with the graphite back gate in order to eliminate the surface roughness of SiO_2 substrate as well as the high-*k* Al_2O_3 deposition. The dominant origin for the interface states is discussed by comparing the subthreshold swing (SS) expressed as

$$SS = \frac{\ln(10)\, k_B T}{e}\left(\frac{C_{it}}{C_{ox}} + 1\right),$$

where C_{it} and C_{ox} are interface states and oxide capacitances, respectively, and $\ln(10)k_BT/e$ is ideal SS value of 60 mV/dec at room temperature.

2. Device fabrication

MoS_2/*h*-BN/graphite device was fabricated on the SiO_2/Si substrate, as shown in **Fig. 1**. First, *h*-BN and MoS_2 crystals were mechanically exfoliated on a polydimethylsiloxane (PDMS) sheet separately. These crystals were transferred on graphite bulk crystal on the SiO_2/Si substrate in the order of *h*-BN and monolayer MoS_2 using the alignment system. Then, this van der Waals (vdW) heterostructure was annealed for 30 minutes at 150 °C. The Ni/Au electrodes were then formed using the electron beam lithography.

The thickness of *h*-BN was measured as ~9.5 nm by atomic force microscopy (AFM). It should be emphasized that the utilization of graphite back gate is critical because the back gate capacitance of *h*-BN insulator can be increased and the effect from charged impurities in SiO_2 can be screened.

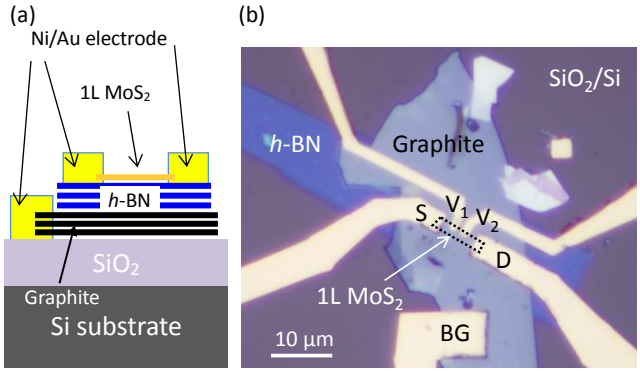

Fig. 1 (a) Schematic illustration (a) and optical image (b) of the MoS_2 vdW heterostructure FET device.

3. Characterization of vdW heterostrcure

First of all, the topography of *h*-BN/graphite on SiO_2/Si substrate was measured by AFM. Histogram of the corresponding height distribution over the 0.5×0.5 μm^2 regions are presented in **Fig. 2(a)**. Compared with the SiO_2/Si substrate, the sharper distribution is evident. The root mean squares (RMS) for *h*-BN and SiO_2 were ~0.05, and ~0.1 nm, respectively.

Photoluminescence (PL) spectra were obtained from monolayer MoS_2 on different substrates, as shown in

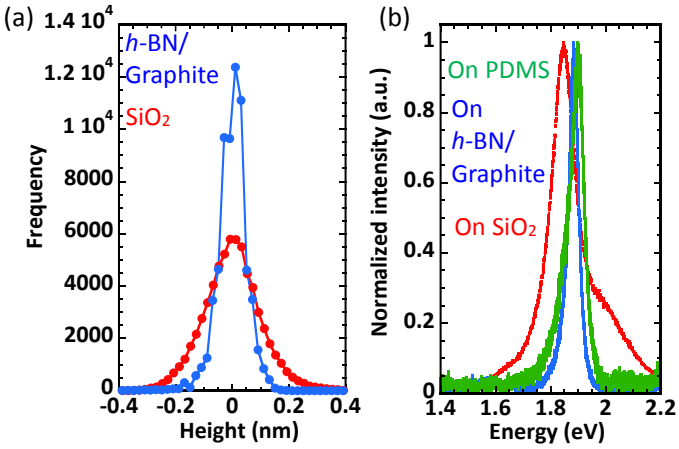

Fig. 2 (a) Height histograms for SiO_2 and *h*-BN/graphite. (b) PL spectra of 1L MoS_2 on different substrate.

Fig. 2(b). The full width at half maximum (FWHM) of the peak for MoS_2 on *h*-BN was 0.07cm^{-1}, which was much narrower than that on SiO_2 (~0.11 cm^{-1}) as well as that on PDMS (~0.10 cm^{-1}). This could be ascribed to the reduction of inhomogeneity by the surface roughness and the charged impurities. The PL peak of the so-called A$^-$ trion around 1.85 eV for MoS_2 on *h*-BN was much weaker than that on SiO_2, suggesting that the electron doping to MoS_2 from *h*-BN was limited compared with that on SiO_2 [2]. As can be seen later, the threshold voltage of MoS_2 on *h*-BN was closer to V_G = 0 V than that on SiO_2. These results indicate that the interaction of MoS_2 with *h*-BN is much reduced from that with SiO_2.

4. Transport properties

Fig. 3 shows the two terminal I_D-V_G characteristics of the device shown in **Fig. 1(b)** at room temperature for the V_G step of 0.005 V. The hysteresis measured at 10^{-11} A was 0.0073 V. The inset shows that the SS value reaches ~80 mV/dec in the range of 10^{-13}~10^{-11} A, indicating the small D_{it}.

Fig. 4 shows the temperature dependence of SS for monolayer MoS_2 on *h*-BN. The SS of 80 mV/dec at room temperature decreased with decreasing the temperature to ~40 mV/dec at 10 K. The slope was close to the ideal case. So far, SS for high-*k*/MoS_2 FET showed no temperature dependence because of large contribution of C_{it} or showed limited temperature dependence. It should be noted that the comparison of SS is possible because C_{ox} for the present *h*-BN is ~0.35 μFcm^{-2} which is comparable with ~0.4 μFcm^{-2} for the high-*k* Al_2O_3 gate insulator.

Finally, **Fig. 5** compares SS for monolayer MoS_2 with different device structures. It indicates that as a whole tendency, SS for MoS_2 on *h*-BN/graphite is

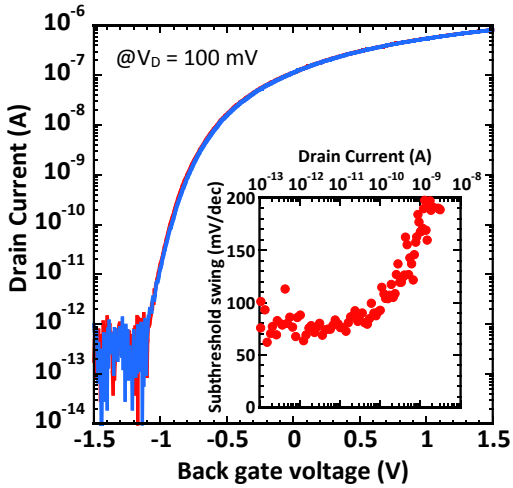

Fig. 3 Transfer characteristics of MoS_2 vdW heterostructure FET at RT. The inset shows SS as a function of drain current.

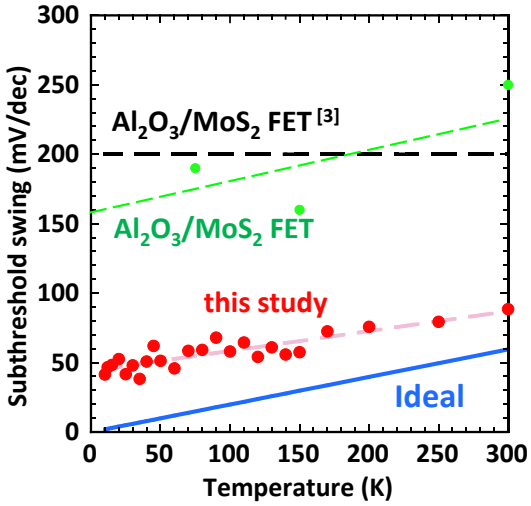

Fig. 4 SS as a function of temperature for MoS_2 vdW heterostructure FET.

lower than that for MoS_2 on SiO_2 with high-*k* gate deposition. On the other hand, when MoS_2 is just transferred on SiO_2 or high-*k* substrate, SS would be relatively small. Moreover, *h*-BN top gate had almost no influences on SS. This comparison clearly indicates that the deposition of high-*k* oxide degrade SS. That is, the strain introduced in MoS_2 due to the deposition would be the dominant origin for the band tail distribution of D_{it}.

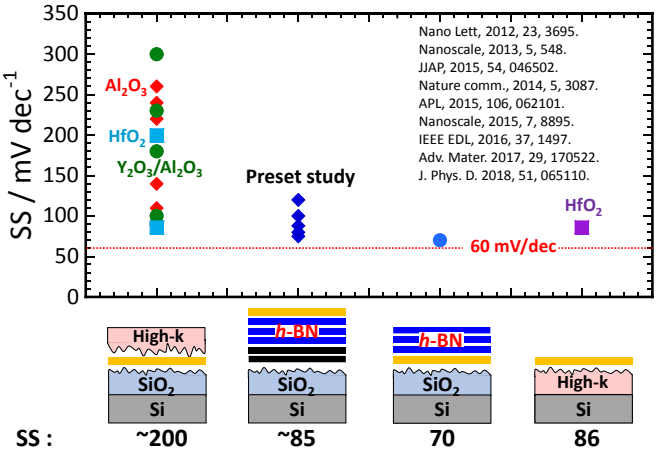

Fig. 5 Comparison of SS for different device structures.

5. Conclusions

The MoS_2/*h*-BN/graphite vdW heterostructure FET was successfully fabricated. Based on the SS comparison for different device structures, the dominant origin for the band tail distribution of D_{it} is suggested to be the strain introduced in MoS_2 during the top gate high-*k* deposition.

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References: [1] N. Fang, K. Nagashio, J. Phys. D, 2018, **51**, 065110.[2] K. Mak *et al.*, nature matt., 2013, **12**, 207. [3] W. Zhu, *et al.*, nature commun., 2014, **5**, 3087.