Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp755-756

p-MoS_2/HfS_2 van der Waals Heterostructure Transistor Using Ni Backgate Buried in HfO_2 Dielectric

Wenlun Zhang[1], Seiko Netsu[1], Toru Kanazawa[1], Tomohiro Amemiya[2], and Yasuyuki Miyamoto[1]

[1] Dept. Electrical and Electronic Engineering, Tokyo Institute of Technology
[2] Institute of Innovative Research (IIR), Tokyo Institute of Technology
2-12-1 Ookayama Meguro-ku
Tokyo 152-8552, Japan
Phone: +81-3-5734-2555 E-mail: zhang.w.ai@m.titech.ac.jp

Abstract

p-MoS_2/HfS_2 van der Waals (vdW) heterostructure transistors were studied. Ni backgate buried in HfO_2 dielectric was introduced for lowering the gate leakage and realizing thinner gate dielectric. Results show that buried gate electrode is one solution to circumvent the gate leakage. By reduction of gate leakage, we could increase gate dielectric capacitance 3 times and subthreshold slope (SS) of 300 mV/dec was achieved.

1. Introduction

The basic principle of semiconductor industry for the past few decades has been the miniaturization of integrated circuits (ICs) by scaling down the metal-oxide field-effect transistors (MOSFETs). However, with the tremendous increases of transistor count, power dissipation of modern ICs become a critical problem to be solved. The conventional MOSFETs, which are restricted by the Boltzmann limit, show the theoretical SS of ~60 mV/dec at room temperature (300 K). To reduce the operating voltage, new switching mechanisms should be explored to break the 60 mV/dec bottleneck for future power-efficient electronics. Extensive research on conventional 3D materials based tunneling field effect transistors (TFETs) with heterojunctions for high on-current has been conducted, but these TFETs suffered from imperfections such as lattice mismatch and trap state at the tunneling surface. Low defect density and sharp band edges are crucial to the quality of heterojunctions, which is important to realize a high performance TFET. In this study, transition metal dichalcogenides (TMDs) are utilized to achieve an atomically perfect interface. In TMDs, MoS_2 and HfS_2 are able to form type-II band alignment with appropriate band offset. Thus, we fabricated p-MoS_2/HfS_2 vdW transistor with a backgate to switch the current toward TFETs [1]. In former trails, we observed the degradation of the SS, probably due to interface traps at the gate interface. Impact of the interface trap can be suppressed by increasing the value of gate dielectric capacitance. Hence, a steep SS can be obtained by enlarging the gate dielectric capacitance. However, reducing the thickness of the gate dielectric gives rise to a severer gate leakage. As we used a global backgate structure, an extra path due to the overlap between the S/D electrode pad and the backgate provide more gate leakage. To lower the gate leakage and investigate the intrinsic subthreshold characteristics, we utilized a Ni backgate buried in HfO_2 gate dielectric in this study.

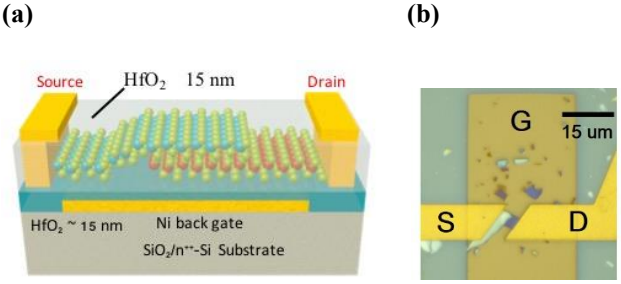

Fig. 1 Device structure of p-MoS_2/HfS_2 vdW heterostructure transistor. **(a)** Schematic view. **(b)** Optical microscope image.

2. Fabrication

Figure 1 (a) shows schematic of the p-MoS_2/HfS_2 vdW heterosturcture transistor, and Fig 1 (b) shows the optical microscope image of the fabricated device. First, gate electrodes were designed using electron beam lithography, and 50 nm Ni was evaporated using electron beam evaporation for deposition on SiO_2/n^{++} Si substrate. After the lift-off process, 15 nm HfO_2 was deposited as gate dielectric by plasma-enhanced atomic layer deposition (ALD). HfS_2 flakes were mechanically exfoliated and transferred to the substrate by Scotch-tape method. Similarly, MoS_2 flakes were transferred to the polydimethylsiloxane (PDMS), and then overlapped with target HfS_2 flake above the gate electrode by the micromanipulator alignment system [2]. Afterwards, S/D electrodes (Ti/Pd/Au: 20 nm/20 nm/80 nm) were formed using electron beam evaporation, and 20nm HfO_2 was deposited by thermal ALD as passivation layer to protect the device from atmospheric contaminants [3]. The device was finally annealed in a vacuum chamber at 250°C for 1 hour to improve its electrical performance [4].

To confirm the effect of reduction of gate dielectric thickness in simple MOSFET, HfS_2 MOSFET in a global backgate structure with 10-nm-thick HfO_2 gate dielectric was also fabricated.

3. Results and Discussion

In our previous work on p-MoS_2/HfS_2 heterostructure transistor, an ON/OFF ratio of 10^4, a maximum drain current over 20 nA and an SS value of 700 mV/dec were observed using a global backgate structure with 25 nm Al_2O_3 gate dielectric [1].

Even in a 2D material MOSFET, the SS is influenced by the interface trap as shown in the equation below [5]. In a TFET also, impact of interface trap can be suppressed by increasing the gate dielectric capacitance.

$$SS = \frac{kT}{q} \ln 10 \cdot (1 + \frac{C_{it}}{C_{ox}}) \qquad (1)$$

However, the simple utilization of a thin dielectric gives rise to a serious gate leakage, as shown in Fig 2 and Fig 3 (a) in case of an HfS_2 MOSFET in a global backgate structure with 10-nm-thick HfO_2 gate dielectric. The gate leakage hindered the observation of subthreshold current. From the optical microscope image, shown in Fig 2, the overlap area between backgate and S/D electrode pad was evaluated to be 9,800 μm^2. The gate leakage at zero gate bias and 2 V drain bias was over 10^{-8} A.

We used a 50 nm Ni backgate buried in the dielectric to reduce the overlap between the S/D electrode and gate electrode and the overlap was evaluated to be around 300 μm^2 in trail of p-MoS_2/HfS_2 heterostructure transistor. The gate dielectric thickness was also selected to be 15 nm HfO_2. In comparison with our previous work, 25 nm Al_2O_3 equivalent oxide thickness (EOT) = 10.8 nm, replaced by 15 nm HfO_2 (EOT = 3.7 nm) still lead to a 3 times increase in the gate dielectric capacitance, which can effectively optimize the device performance in spite of the interface trap. The transfer characteristic of the p-MoS_2/HfS_2 heterostructure transistor is shown as Fig 3 (b), the ON/OFF ratio is beyond 10^4 and the lowest SS is reduced to 300 mV/dec. By increasing the oxide thickness by 5 nm and reducing over 97% overlap area, the gate leakage current was effectively suppressed to around 10^{-12} A.

4. Conclusions

In this report, we fabricated p-MoS_2/HfS_2 vdW heterostructure transistors. As reduction of EOT lead to trends of gate leakage, we utilized a buried backgate structure to resolve this problem. The results of the experiment showed that increasing the value of gate dielectric capacitance suppresses the influence of interface trap, which results in improved subthreshold characteristics.

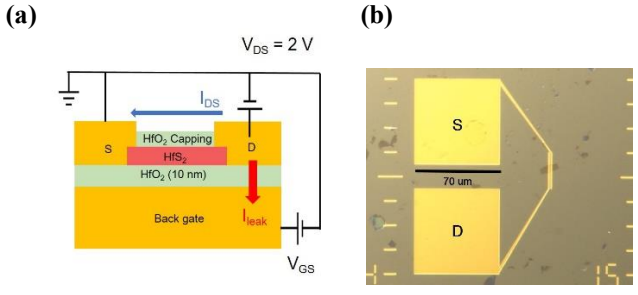

Fig. 2 (a) Schematic view of a 10 nm HfO_2 gate dielectric HfS_2 MOSFET in a global backgate structure. **(b)** Optical microscope image.

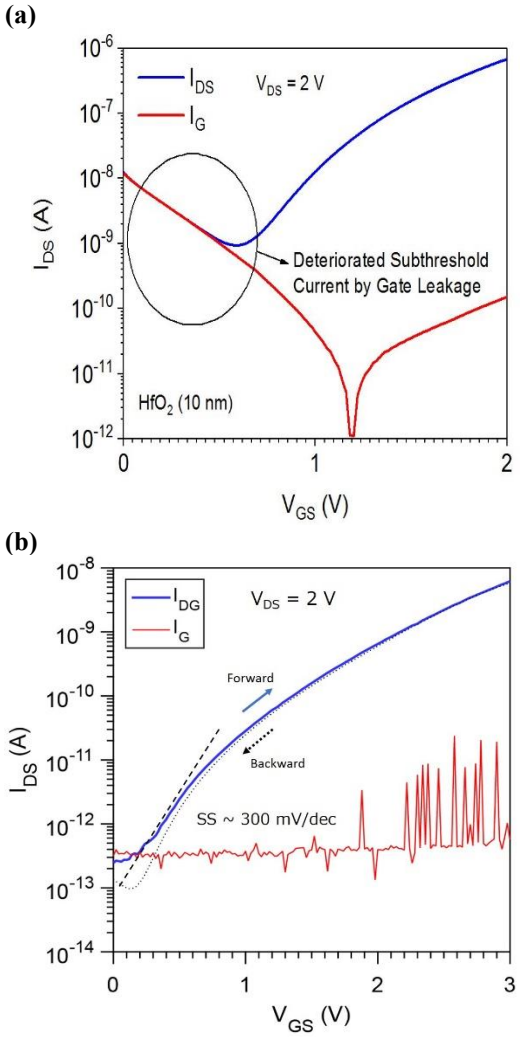

Fig. 3 (a) Transfer characteristics of a 10 nm HfO_2 gate dielectric HfS_2 MOSFET in a global backgate structure. **(b)** Transfer characteristics of 15 nm HfO_2 gate dielectric p-MoS_2/HfS_2 heterostructure transistor.

Acknowledgements

This work was supported by JSPS KAKENHI Grant Number JP18K04279, JP16H00905 and JP25107004, and Tokyo Institute of Technology Ookayama Materials Analysis Division.

References

[1] S.Netsu, T. Kanazawa, T. Uwanno, T. Amemiya, K. Nagashio and Y. Miyamoto, To be published in IEICE Trans. Electron. (2018)

[2] T. Uwanno, Y. Hattori, T. Taniguchi, K. Watanabe and K. Nagashio, 2D Mater. **2** (2015) 041002

[3] T. Kanazawa, T. Amemiya, V. Upadhyaya, A. Ishikawa, K. Tsuruta, T. Tanaka and Y. Miyamoto, IEEE Trans. Nanotechnology **4** (2017) 16

[4] V. Upadhyaya, T. Kanazawa, and Y. Miyamoto, IEICE Trans. Electron. **E100-C** (2017) 453

[5] T. Li, B. Wan, G. Du, B. Zhang and Z. Zeng, AIP Advances **5** (2015) 057102