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High Performance Monolithic Complementary Integrated Circuits Based on 2D Black Phosphorus/HfO_2 Heterostructure

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ABSTRACT

We demonstrate a monolithic integration strategy for realizing complementary black phosphorus (BP) transistors and integrated circuits with HfO_2 high-κ gate dielectric. For a low supply voltage V_{DD} of 1.5 V, a high voltage gain of ~11 is achieved in our BP inverter circuit. Simultaneously, a symmetrical noise margin of 0.27 V_{DD} is measured for both low and high input voltages, showing good immunity to input signal noise. In addition, a three-stage ring oscillator is theoretically examined by circuit modeling based on the device measurements, showing an oscillation frequency above 1.8 GHz at a micro-watt level power dissipation, showing promise for cascaded circuit applications.

INTRODUCTION

BP is a promising two-dimensional (2D) layered material for nanoelectronic applications due to its superior carrier mobility and finite bandgap over graphene and other transition metal dichalcogenides (TMDs) [1]. Numerous field-effect transistors (FETs) based on BP have been reported recently [2-4] which predominantly demonstrated p-type characteristics. Moreover, due to the lack of reliable doping technique, the reported BP inverters are primarily realized using hybrid integration approach which employ two different 2D channel materials [3,5-10] that requires complicated transfer and external wiring process, making it impractical and costly to implement for large scale manufacturing. The realization of a truly monolithic 2D integrated circuit remains elusive.

In this work, we employ a reliable aluminum (Al) doping technique to convert p-type BP into n-type conductivity, thereby enabling complementary inverter circuit to be demonstrated on a single BP channel material. The complementary inverter achieves a voltage gain of ~11 at V_{DD} = 1.5 V and a noise margin of 0.27 V_{DD} for both low and high input voltages, showing good immunity to input noise. A three-stage ring oscillator with an oscillation frequency above 1.8 GHz and a low power dissipation is theoretically modelled, showing great potential for complex logic circuit applications.

DEVICE FABRICATION

Fig. 1 shows the schematic structure of the monolithically integrated BP complementary inverter. 4" heavily doped p-type silicon wafer is employed as the conducting back gate electrode. A 20 nm HfO_2 is deposited on the substrate using ALD at 120 °C. After that, 5 nm Ti/ 60 nm Au and 5 nm Ni/ 60 nm Au are deposited as the metal electrodes for n-type FET and p-type FET, respectively, using e-beam evaporation. After a standard lift-off process, a square area on the channel of BP n-FET is exposed by e-beam lithography. Finally, Al dopants are doped into the BP flake using TMA precursor by ALD process at 120 °C. Fig. 2 shows the monolithic integration process flow and the optical image of the completed BP complementary inverter is shown in Fig. 3.

RESULTS AND DISCUSSION

A. Characteristics of Complementary BP Field-Effect Transistors

Electrical measurements are performed under atmospheric environment at room temperature. The typical I_D-V_D curves of p-type and n-type transistors are shown in Fig. 4 and Fig. 5, respectively. Fig. 6 shows the I_D-V_G curves of both p-type and n-type BP transistors. Symmetric threshold voltages are achieved by tuning the Al doing concentration in the BP n-FET. A thin high-κ gate dielectric of ~20 nm is employed to reduce the subthreshold swing *SS* to ~287.5 mV/dec, showing significant improvement over other reported BP transistors with SiO_2 as the gate dielectric (high *SS* of ~1 V/dec). Fig. 7 shows the extracted contact resistance using first-order exponential fitting method. Metal work function engineering is employed to reduce the contact resistance of BP FETs, in which nickel (Ni) and titanium (Ti) are favorable metal electrodes for p-FET and n-FET, respectively. Additionally, the hole and electron field-effect mobilities are ~170 $cm^2/V{\cdot}s$ and ~25 $cm^2/V{\cdot}s$, respectively (Fig. 8). By decoupling the effect of contact resistance, the intrinsic mobility for holes and electrons are enhanced to ~342 $cm^2/V{\cdot}s$ and ~117 $cm^2/V{\cdot}s$, respectively.

B. Characteristics of BP Complementary Inverter

Fig. 9 shows the output voltage as a function of input voltage at V_{DD} = 1 V, 1.5 V, and 2 V, respectively. An ideal switching threshold voltage of ~0.5 V_{DD} = 0.75V is achieved at V_{DD} = 1.5V, suggesting the well symmetrical characteristic of the inverter. The voltage gain (defined as dV_{out} / dV_{in}), which indicates the sensitivity of V_{out} changed by V_{in}, is extracted to be 9, 11 and 13, at V_{DD} = 1 V, 1.5 V and 2 V, respectively, as shown in Fig. 10. Additionally, the noise margin of high input voltage is extracted to be $NM_H \approx 0.27$ V_{DD}, while the noise margin of low input voltage is $NM_L \approx 0.27$ V_{DD} for a V_{DD} = 1.5 V (Fig. 11). The high noise margin indicates that the inverter has a good immunity to input signal noise and can be used to build more complex logic circuits. A benchmarking of complementary inverters using BP as the channel material is shown in Fig. 12. Our BP complementary inverter achieves a relatively high voltage gain at a low supply voltage as compared with other hybrid inverters requiring either a transfer process or an external wire bonding, indicating that our study demonstrates a more practical method to fabricate high performance logic circuits using single BP as the channel material.

C. Three-Stage BP Complementary Ring Oscillator

The performance of a three-stage ring oscillator is theoretically examined by circuit modeling. Based on the I_D-V_D experimental data of p-type FET and n-type FET (Fig. 4 and Fig. 5), we create the SPICE models for both the FET devices, which are used to build a complementary inverter. The simulated results show good agreement with the measured characteristics. A ring oscillator is composed of an odd number (three stages in this work) of inverter in a ring. The inset on the right bottom of Fig. 13 gives a 3-stage oscillator circuit diagram, where *C* is the equilibrium parasitic capacitance for each stage. Given V_{DD} = 1.5 V and *C* = 1 nF, output characteristics (Fig. 13) of the oscillator shows an oscillating frequency of 1.8 GHz and a voltage swing of 1 V (from 0.3 V to 1.3 V). When the equilibrium parasitic capacitance *C* is varied from 0.1 nF to 1 nF, the oscillating frequency is increased from 1.8 GHz to 18 GHz (Fig. 14), thus showing a negative correlation with parasitic capacitance and indicating a higher frequency can be achieved by optimizing the metal electrode patterns. Fig. 15 shows the oscillation frequency and power dissipation as a function of power supply. High oscillation frequency of >1 GHz can be achieved at a low power supply. Fig. 16 shows the benchmarking of reported ring oscillators in terms of power supply and various channel materials such as Si, graphene, CNT etc.[11-16]. Compared with other oscillators, BP-based oscillator has the lowest propagation delay of ~0.2 ns per stage for a low power supply of <2 V, which exemplifies the potential of BP as an emerging channel material for logic circuits applications.

CONCLUSION

Complementary black phosphorus inverter circuits built on high-κ gate dielectric with high voltage gain and noise margin are successfully demonstrated *via* a monolithic integration strategy. Moreover, a three-stage ring oscillator with a high frequency above 1.8 GHz and micro-watt level power dissipation is theoretically achieved at a low supply voltage. This work demonstrates a practical approach to realize complementary transistors and circuits on a homogenous BP channel material, paving the way towards complex cascaded circuit applications.

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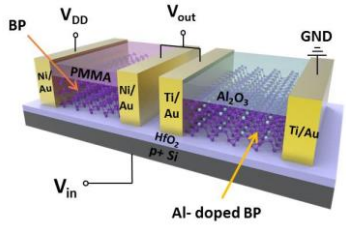

Fig. 1. Three-dimensional structure of BP complementary inverter circuit. Conductivity of BP is transformed from p-type to n-type using Al doping.

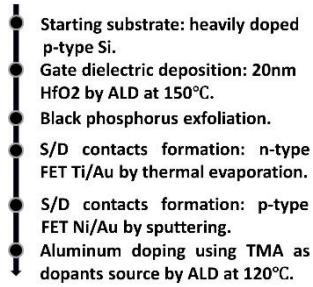

Fig. 2. Monolithic integration flow for realizing complementary black phosphorus transistors and circuits.

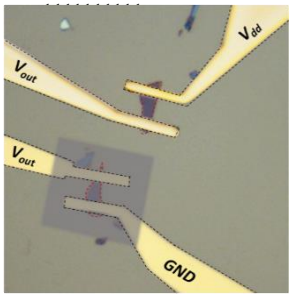

Fig. 3. Optical image of BP complementary inverter. The grey area is the region with Al-doping.

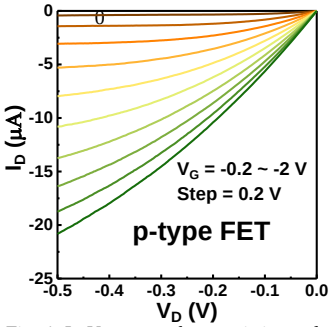

Fig. 4. I_D-V_D output characteristics under different V_G from -0.2 V to -2 V with a step of -0.2 V of p-type BP FET.

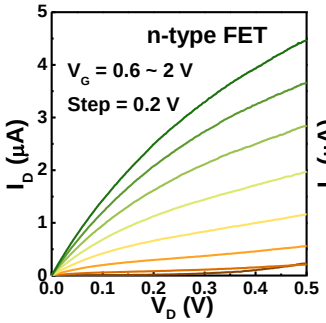

Fig. 5. I_D-V_D output characteristics under different V_G from 0.6 V to 2 V with a step of 0.2 V of n-type BP FET.

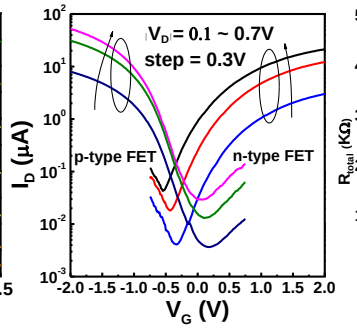

Fig. 6. I_D-V_G curve under different $|V_D|$ from 0.1 V to 0.7 V with a step of 0.3 V for p-type and n-type BP FET. Symmetric transistors are achieved by threshold voltage tuning.

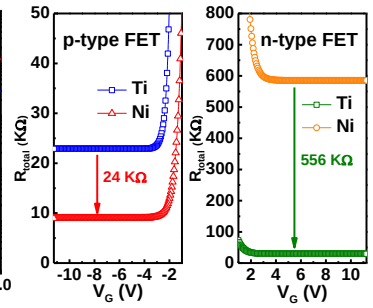

Fig. 7. Contact resistance using different metal as the metal electrodes for different transistors. Contact resistance is much smaller using Ni and Ti for p-FET and n-FET, respectively.

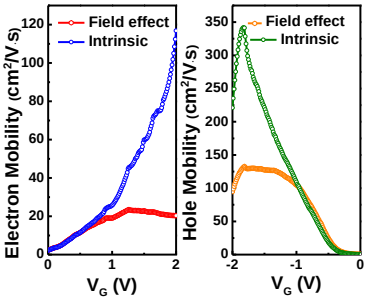

Fig. 8. Carrier mobility extraction shows an intrinsic mobility of ~117 cm^2/V·s and 342 cm^2/V·s for electron and hole, respectively.

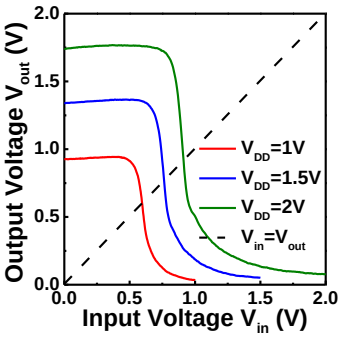

Fig. 9. The output voltage as a function of input voltage of the BP complementary inverter under different supply voltage from 1 V to 2 V with a step of 0.5V. V_M = 0.75 V at V_{DD} = 1.5 V is achieved, which is near to the ideal V_M = 0.5 V_{DD}.

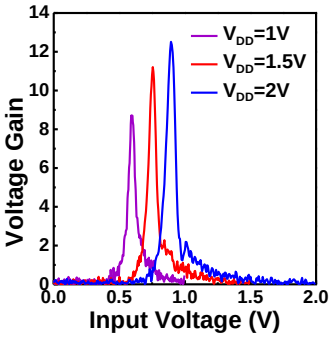

Fig. 10. Voltage gain as a function of input voltage of the BP complementary inverter under different supply voltage from 1 V to 2 V with a step of 0.5 V. The voltage gain is up to ~13 for a V_{DD} of 2 V.

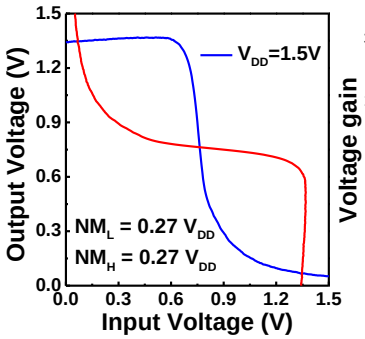

Fig. 11. Extracted noise margin at low and high input voltages. Both the noise margin low (NM_L) and noise margin high (NM_H) are up to 0.27 V_{DD}, showing a good noise immunity which renders it suitable for complex circuits manufacturing.

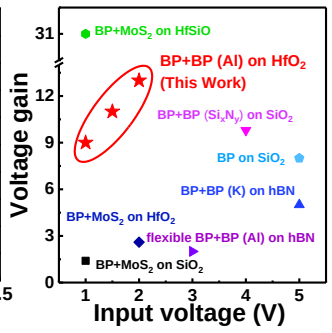

Fig. 12. Performance benchmarking of complementary inverters using black phosphorus as the channel material. Our work achieves a low voltage gain alongside a low supply voltage.

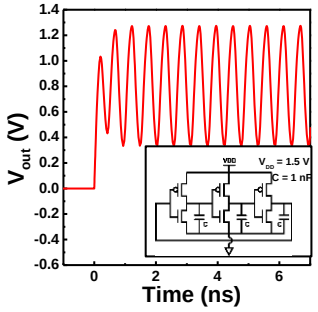

Fig. 13. Output characteristics of the BP ring oscillator with an oscillating frequency of 1.8 GHz and a voltage swing of 1 V for a given V_{DD} of 1.5 V; The inset on the bottom right shows a 3-stage ring oscillator circuit diagram.

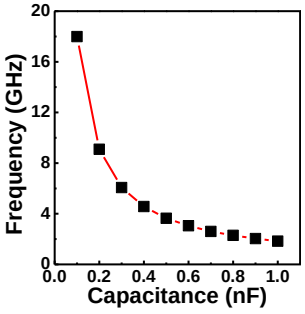

Fig. 14. Oscillation frequency increases monotonically as the parasitic capacitance reduces, which can be achieved by optimizing the device structure, showing the potential to achieve even higher frequency.

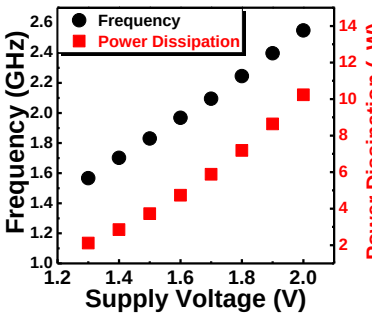

Fig. 15. Oscillation frequency and power dissipation as a function of power supply. Reducing the supply voltage leads to a reduction of power dissipation, while still yields an oscillation frequency above 1 GHz.

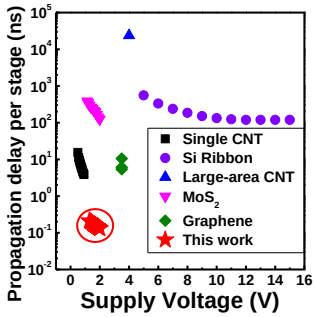

Fig. 16. Benchmarking of propagation delay per stage versus supply voltage for ring oscillators made of various semiconductor materials. Our BP ring oscillator achieves the lowest propagation delay time at a low power supply < 2 V.

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