Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp761-762

High-k Er_2O_3 top gate deposition on 2D channel at room temperature by P_{O2} controlled thermal evaporation

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Abstract: By introducing the differential-pressure-type deposition chamber, the high quality Er_2O_3 dielectrics were deposited on 2D channel at the room temperature at different P_{O2} condition. We demonstrate the top gate capacitance of 1.14 μF/cm² by analyzing the I-V data for dual-gate graphene FET.

1. Introduction

The high-k gate stack formation on 2 dimensional (2D) layered channels is often formed by atomic layer deposition (ALD) with the assistance of buffer layers [1-3]. However, there are two major problems. First, the quality of ALD high-k film is substantially degraded due to the low quality of the buffer layers. Second, the substrate temperature in ALD is generally increased to 200 °C in the oxidant vapor environment. This deposition condition cannot be applied to vulnerable 2D materials typically with low melting points. Alternatively, we have fabricated the high quality Y_2O_3 on graphene by the thermal deposition of rare earth Y metal under the controlled oxygen partial pressure (P_{O2}) and subsequent high pressure O_2 annealing at 300 °C [4]. Although this Y_2O_3 film showed superior dielectric breakdown behavior > 1 V/nm, it suffered from the high surface roughness because the high deposition rate of ~5 nm/s was necessary to avoid the oxidation of the Y feed metal.

In this study, we have introduced differential-pressure-type deposition chamber, in which the feed source and the deposition chambers are separated by an aperture of ϕ = 5 mm and can be evacuated independently, as shown in **Fig 1**. In this study, by controlling the deposition condition such as deposition rate, P_{O2} and temperature, the insulator properties are evaluated by the I-V measurement.

2. Optimization of deposition condition on Si

In this study, Er_2O_3 with k = ~13 was selected as high-k insulator instead of Y_2O_3 because the feed source temperature can be kept low by its higher vapor pressure. When P_{O2} in the deposition chamber was adjusted to 10^{-2} Pa, P_{O2} in the feed source chamber could be maintained below 10^{-5} Pa. Because of high vacuum condition in the feed source chamber, the deposition rate of ~0.04 Å/s was achieved at 1080 °C. To optimize the deposition condition, Er_2O_3 with 10 nm in thickness was deposited on p-Si substrate at different P_{O2} and at the room temperature (RT). The thickness of Er_2O_3 film was determined by the grazing incidence X-ray reflectivity measurement. Then, MOS capacitor structure with Au top and Al bottom electrodes were fabricated for the electrical measurement.

Figure 2 shows the breakdown field obtained by I-V measurement and the dielectric constant estimated by C-V measurement for the range of $10^{-5} \leq P_{O2} \leq 10^{-1}$ Pa. The former gradually increases with increasing P_{O2}, while the latter clearly shows the maximum at $P_{O2} = 10^{-2}$ Pa, which is higher than that for Y_2O_3. Furthermore, the maximum P_{O2} also shifts to low pressure region. These results suggest that the film quality is improved by the lower deposition rate.

3. Characterization of Er_2O_3 on graphene

Next, in order to demonstrate the top gate Er_2O_3 gate stack formation on graphene, monolayer graphene back gate field effect transistors on SiO_2 (90 nm)/n^+-Si substrate are fabricated by the mechanical exfoliation of Kish graphite. Then, Er_2O_3 with the typical thickness of 3-7 nm was deposited on graphene at the optimized condition at $P_{O2} = 10^{-2}$ Pa. Finally, Al top electrode was

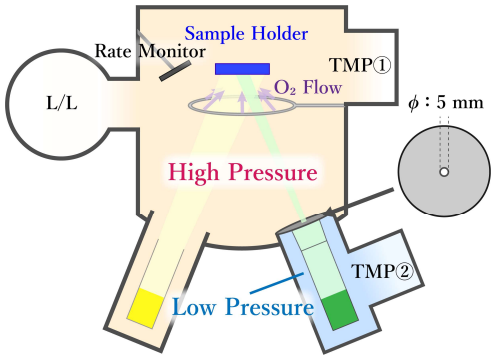

Fig. 1 Differential-pressure-type deposition chamber.

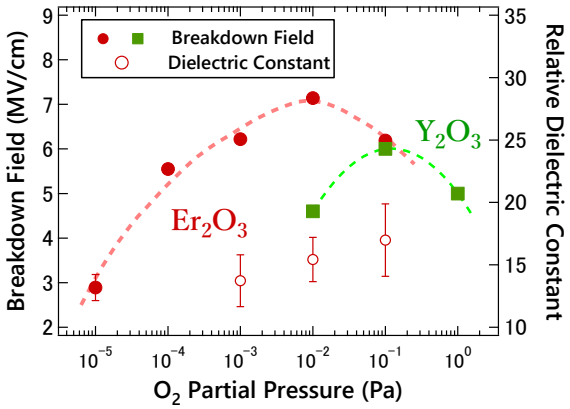

Fig. 2 Breakdown field and dielectric constant vs P_{O2}.

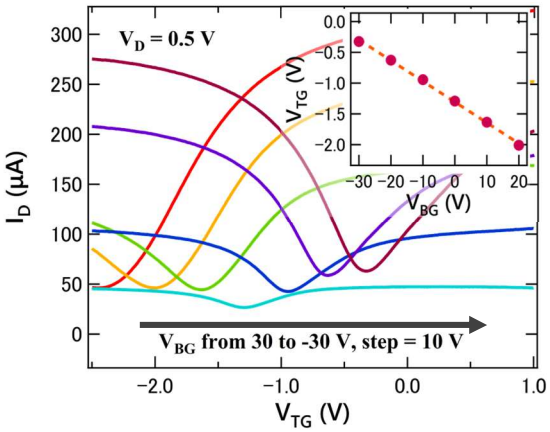

Fig. 3 *I-V* curves as a function of V_{TG}. The inset represents the Dirac point shift as a function of V_{BG}.

formed.

First of all, the surface roughness of Er_2O_3 with 6 nm thickness on bulk graphite was confirmed to be RMS < 0.1 nm. This is much flatter than that of SiO_2 surface (RMS = ~0.2 nm) because of the low deposition rate.

Figure 3 shows the I_D-V_{TG} transfer characteristics of graphene FET with 3.6-nm Er_2O_3 top gate insulator. Clear ambipolar behavior is observed. The inset shows the trace of Dirac point observed at different V_{BG}, where the slope corresponds to the capacitance coupling ratio of back and top gate, i.e., $-C_{BG}/C_{TG}$. Since C_{BG} is 0.038 μF/cm^2 for the 90-nm SiO_2 with k_{SiO2} = 3.9, C_{TG} can be estimated to be 1.14 μF/cm^2 with 3.6 nm thickness. Then, the dielectric constant of Er_2O_3 on graphene is calculated as ~5, which is much smaller than that on Si. The reduction in dielectric constant on 2D materials has also been observed in ALD, as shown in **Fig. 4**. On the other hand, the dielectric breakdown field was estimated as 8.3 MV/cm, which is higher than that on Si, as shown **Fig. 5**. Thanks to the surface flatness of Er_2O_3, quite thin thickness of Er_2O_3 as well as high dielectric breakdown field was achieved.

Finally, let us discuss the film quality in terms of $D_{max} = V_{max}C_{TG}/\epsilon_0$, which is the maximum vertical electrical field applied to 2D channels. For various bi

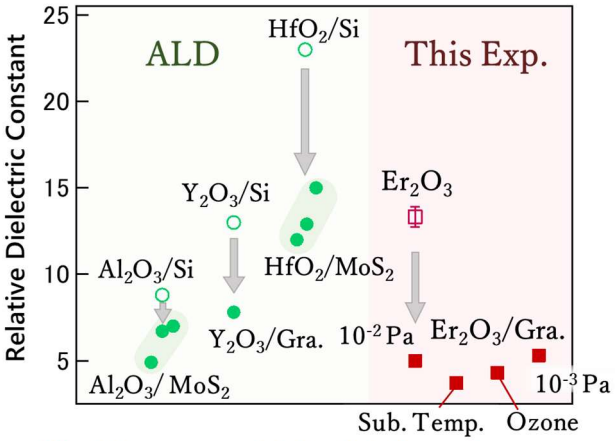

Fig. 4 Comparison of relative dielectric constants.

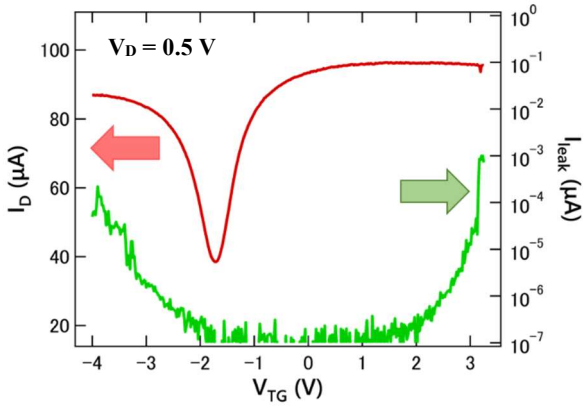

Fig. 5 I_D-V_G curve and I_G-V_G at V_{BG} = 0 V for 3.6-nm Er_2O_3 top gate graphene FET.

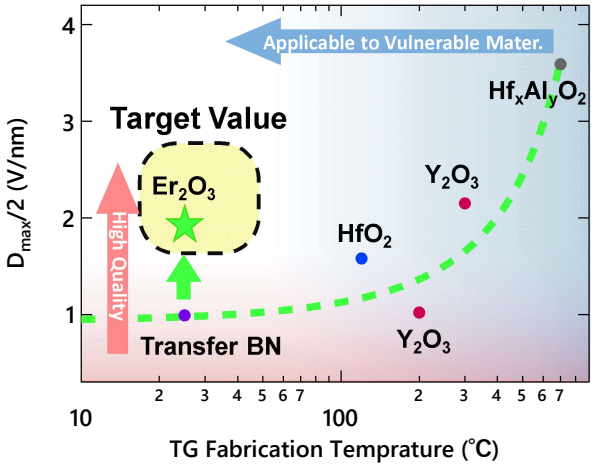

Fig. 6 D_{max} as a function of the deposition temperature for high-*k* on graphene. The literature data in which the defects are introduced in graphene are omitted here.

layer 2D materials, it is known that the band gap (E_G) can be reduced by applying D and closed completely at D = ~3 V/nm [5]. Here, since the present Er_2O_3 shows $D_{max}/2$ = 1.9 V/nm, the dual gate structure with back gate provides total D_{max} = ~3.2 V/nm. As shown in **Fig. 6**, the advantage of the present study is that high D_{max} is attained by the RT deposition, suggesting that the present Er_2O_3 can be used to all the vulnerable 2D channels with low melting points.

4. Conclusions

P_{O2} controlled thermal evaporation at RT provided D_{max} = ~3.2 V/nm, suggesting that the present Er_2O_3 can be used to all the vulnerable 2D channels with low melting points.

Acknowledgements: This research was partly supported by the JSPS Core-to-Core Program, A. Advanced Research Networks, JSPS KAKENHI Grant Numbers JP16H04343, Japan.

References: [1] Seong-Jun J. *et al.*, *Sci. Rep.* **6,** 20907 (2016). [2] Yunseong L. *et al.*, *ACS Nano* **10,** 6659 (2016). [3] Takahashi N. *et al.*, *Nanotechnology* **26,** 175708 (2015). [4] Kanayama K. *et al.*, *Appl. Phys. Lett.* **104,** 083519 (2014). [5] Ramasubramaniam A. *et al.*, *Phys. Rev. B* **84,** 205325 (2011).