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Improving hole mobility of solid-phase crystallized Ge on glass by reduction of carrier scattering factors

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Abstract

Polycrystalline Ge thin films are fabricated on glass by solid-phase crystallization. The control of the atomic density of the precursor enlarged the grain size and reduced the barrier height of the grain boundary. By combining post annealing and a GeO_2 underlayer insertion, the hole mobility of Ge reached 570 cm^2/Vs, the highest mobility of semiconductor films grown on insulator at low-temperature (< 900 °C).

1. Introduction

Ge on insulator (GOI) technology has been widely studied for lowering the fabrication cost and improving the device performance of Ge metal-oxide-semiconductor field-effect-transistors. Solid-phase crystallization (SPC) is a simple method to directly form polycrystalline Ge (poly-Ge) thin films on glass substrates at low temperatures [1]. Recently, we improved the hole mobility of SPC-Ge from 140 cm^2/Vs to 340 cm^2/Vs by preparing an amorphous Ge (a-Ge) precursor with heating the substrate [2]. This hole mobility was the highest ever recorded for a thin film formed on insulators at temperatures below the melting point of Ge (937 °C). In this study, we investigated the effects of film thickness, post annealing (PA), and underlayer insertion on the SPC-Ge and broke the record with a hole mobility of 570 cm^2/Vs.

2. Experimental Procedures

In the experiment, the Ge precursors were deposited on SiO_2 glass substrates using the Knudsen cell of a molecular beam deposition system (base pressure: 5×10^{-7} Pa). The thickness of the a-Ge layer, t, ranged from 50 to 500 nm. The substrate temperature during the deposition, T_d, ranged from 50 to 200 °C. The samples were then loaded into a conventional tube furnace in a N_2 atmosphere and annealed at 450 °C for 5 h to induce SPC. After that, we performed post annealing (PA) at 500 °C for 5 h to enhance the electrical properties. A 50 nm-thick GeO_2 underlayer was prepared on the substrate by RF sputtering.

After annealing for SPC, the grown Ge layers were evaluated by using electron backscattering diffraction (EBSD) analysis. The electrical properties of the SPC-Ge layers were evaluated using Hall effect measurements.

3. Results and Discussion

The EBSD images in Fig. 1(a) show that the grains are randomly oriented and the grain size strongly depends on both T_d and t. Fig. 1(b) shows that there are optimum values for both T_d and t. For each t, the grain size expands with the increase of T_d, then turns to shrink. This result suggest that growth rate strongly depends on T_d. As a result, the grain size reaches the highest value at around $100 \leq T_d \leq 150$ °C.

All samples showed p-type conduction, similar to conventional non-doped poly-Ge. This is because point defects in Ge provide shallow acceptor levels and then generate holes at room temperature. Fig. 2(a) shows that hole concentration decreases with increasing t for $T_d = 50$ °C. For $t = 50$ and 100 nm, the hole concentrations are reduced for $T_d > 50$ °C. These behaviors suggest that the point defects located at the interface between Ge and SiO_2 are reduced by the heating deposition of the precursor. For $T_d > 75$ °C, the hole concentration increases as T_d increases for each t. This behavior can be explained from the perspective of the point defects located at grain boundaries and within grains. Since the grain boundary decreases as the grain size increases, point defects due to grain boundaries decrease. On the other hand, in crystal growth, as the growth rate increases, vacancies are more easily taken into the grain. As a result of the balance between the defects in the grain boundary and grain, the hole concentration behaves as shown in Fig. 2(a) with respect to T_d (> 50 °C).

Fig. 2(b) shows that the hole mobility of the SPC-Ge layer strongly depends on T_d, except $t = 50$ nm. For $t \geq 100$ nm, the high hole mobilities (> 250 cm^2/Vs) at $100 \leq T_d \leq 150$ °C are attributed to both the large grain size and low potential barrier height of grain boundaries. The thicker t tends to provide the higher hole mobility despite the grain becoming smaller. These results suggest that the higher hole mobility with the thicker Ge layer arises from the reduction of the interface scattering.

PA were performed for the samples of the highest hole mobility with each t. Fig. 3 shows that the hole concentration decreases for all samples. This result suggests that point defects, generating holes, in the Ge layers were passivated. This increased the hole mobility of all samples.

For further improving the hole mobility, a GeO_2 underlayer was prepared on the substrate. As plotted in Fig. 4, the highest hole mobility was updated to 570 cm^2/Vs. This is because of the reduction of the hole concentration, i.e., impurity scattering, achieved by reduction of the interfacial defects between Ge and the underlayer.

4. Conclusion

We further improved the hole mobility of the SPC-Ge layer by controlling T_d (50–200 °C) and t (50–500 nm), then applying PA (500 °C, 5 h) and preparing a GeO_2 underlayer. The resulting hole mobility, 570 cm^2/Vs, is the highest value to date among that of semiconductor layers

directly formed on glass. This technique will facilitate realization of high-speed thin film transistors and multi-functional devices on insulating substrates.

References

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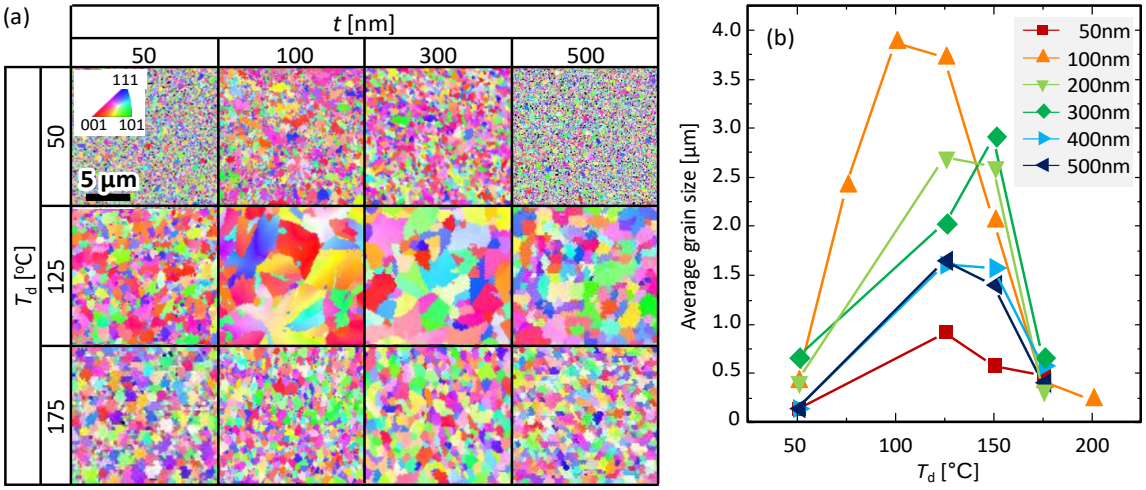

Fig. 1 (a) EBSD images of the samples where T_g = 450 °C. (b) T_d dependence of the grain size obtained from the EBSD analyses.

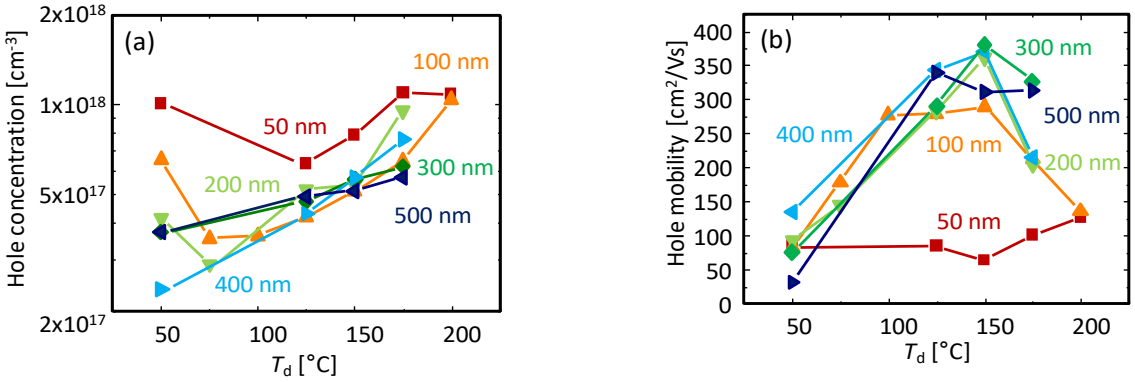

Fig. 2 Electrical properties of the SPC-Ge layers before PA for t = 50-500 nm, obtained by Hall Effect measurement with the van der Pauw method. (a) Hole mobility and (b) hole concentration as a function of T_d.

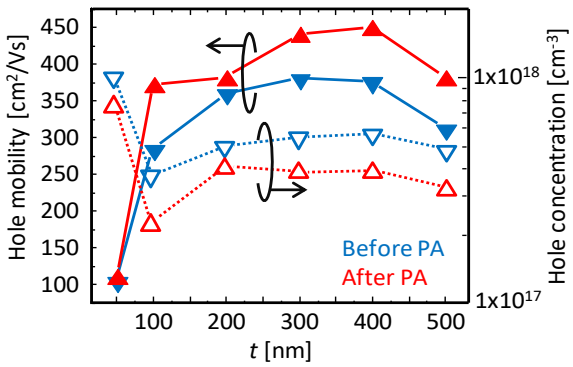

Fig. 3 Hole mobility and hole concentration of the SPC-Ge layers for t = 50-500 nm before and after PA at 500 °C.

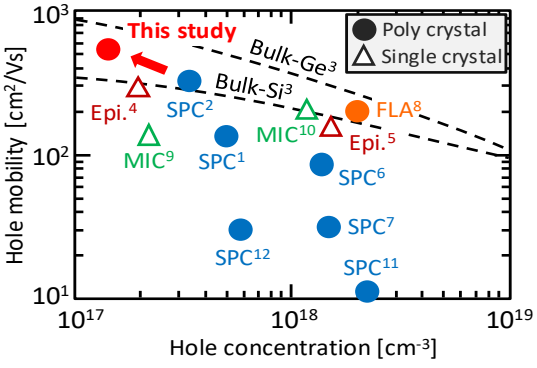

Fig. 4 Comparison of the hole mobility and hole concentration of GOIs.