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High-temperature Electrical Characteristics of 60nm CAAC-IGZO FET: Comparison with Si FET

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Abstract

A c-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO, a crystalline oxide semiconductor) FET with a channel length of 60nm was fabricated to measure electrical characteristics at high temperatures, and demonstrates that the electron mobility is not lowered. This proves that a CAAC-IGZO FET is more suitable for high-temperature use than a Si FET. On the assumption of operation for memory application, the write time and retention time at 192°C are estimated at 0.49ns and 11s, respectively. A CAAC-IGZO FET achieves long retention time under high-temperature conditions, at write speed higher than that with a Si FET.

1. Introduction

Application of c-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO) FETs to LSI as well as displays has been widely studied and developed [1–5]. A CAAC-IGZO FET features in short-channel effect immunity in addition to ultralow off-state current [6], and thus is particularly fit for miniaturization, such as memory application [7, 8]. High temperatures cause characteristics deterioration of a Si FET, such as lower electron mobility and higher leakage current [9]. In contrast, a CAAC-IGZO FET has few factors in characteristics degradation in high-temperature environment [10].

In this report, we fabricated a CAAC-IGZO FET with a channel length (L) of 60nm and measured its temperature dependence in the range of 27 to 192°C. We also measured temperature dependence of a Si FET and assessed the effectiveness of application of the CAAC-IGZO FET to memory in high-temperature environment.

2. Fabricated CAAC-IGZO FET

Fig. 1 shows cross-sectional images of the CAAC-IGZO FET we fabricated this time. The FET has a trench-gate self-aligned structure. The CAAC-IGZO serving as the active layer is formed so that its side surfaces are covered with a Fin-shaped gate electrode. Covering the sides of the active layer facilitates application of gate electric fields to the active layer. A back gate electrode (BGE) is formed at the bottom of the FET [11]. The FET having the BGE enables its threshold voltage (V_{th}) to be adjusted by the BGE voltage. Consequently, the FET has wide applicability to memory because it is capable of adopting various types of driving depending on purpose (e.g., for long retention time or for high speed).

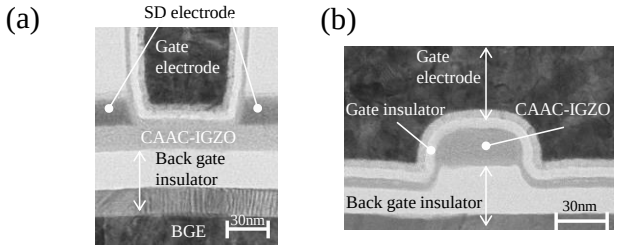

Fig. 1 Cross section of CAAC-IGZO FET in channel length direction (a) and in channel width direction (b).

3. Temperature Dependence of CAAC-IGZO FET

I_d-V_g characteristics of our CAAC-IGZO FET and a bulk Si FET were measured with temperatures varying from 27 to 192°C. Table I presents device parameters of the evaluated FETs.

Table I Parameters of CAAC-IGZO FET and Si FET

	CAAC-IGZO FET	Si FET
Length	60nm	60nm
Width	60nm	120nm
GI thickness	EOT 6.4nm	EOT 2.6nm
Vdd	3.3V	1.2V

First, Fig. 2 shows the temperature dependence of the I_d-V_g curves of the CAAC-IGZO FET and Si FET. For the measurement conditions, the drain voltage was 1.2V for both the FETs, and the highest gate voltage was 3.3V for the CAAC-IGZO FET and 1.2V for the Si FET because of the difference in device withstand voltage.

The V_{th} of both these FETs is shifted more negatively at higher temperatures. As shown in the graph, the CAAC-IGZO FET having a substrate-on-insulator structure is less likely to be affected by the punch-through effect via the substrate caused when the gate voltage is negative.

Next, Fig. 3 shows the temperature dependence of saturation mobility. The saturation mobility of the Si FET becomes lower at a higher temperature; whereas in the CAAC-IGZO FET, the saturation mobility is not lowered at

high temperatures, and variations in saturation mobility are small in the range between 27 and 192°C.

Fig. 4 presents the temperature dependence of off-state current and the temperature dependence of the ratio of on-state current to off-state current. The off-state current was calculated with a drain voltage of 1.2V and a gate voltage of 0V. The off-state current of the CAAC-IGZO FET is below the detection limit and thus was determined by extrapolation of the subthreshold slope and V_{th} [10]. The on-state current of the CAAC-IGZO FET was measured at a gate voltage of 3.3V and a drain voltage of 1.2V; that of the Si FET was measured at a gate voltage and a drain voltage of 1.2V. The CAAC-IGZO FET exhibits an extremely high on/off ratio and has an on/off current ratio on 11 orders of magnitude at 192°C.

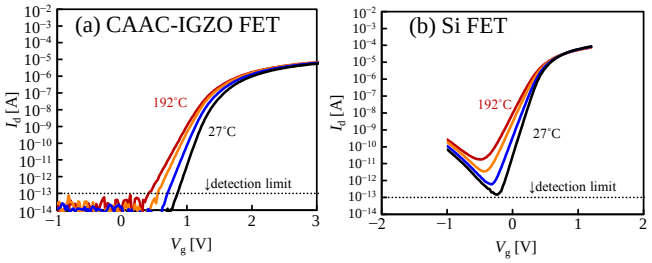

Fig. 2 Temperature dependence of I_d-V_g curves of CAAC-IGZO FET (a) and Si FET (b).

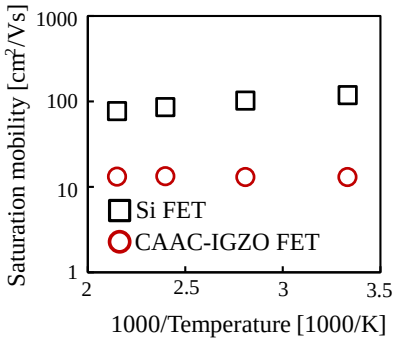

Fig. 3 Temperature dependence of saturation mobility.

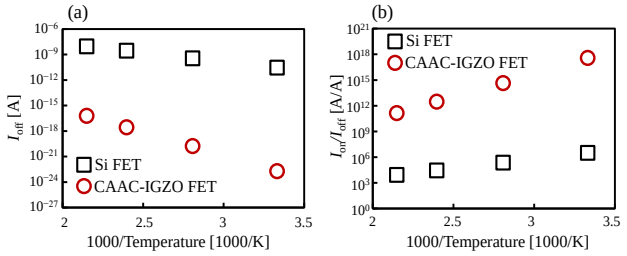

Fig. 4 Temperature dependence of drain current; (a) off-state current and (b) ratio of on-state current to off-state current.

4. Application of CAAC-IGZO FET to Memory

An example of a 1Tr1C (like DRAM) memory cell adopting a CAAC-IGZO FET is dynamic oxide semiconductor random access memory (DOSRAM) [3, 4, 12]. The write speed and retention time were calculated using a TEG assuming the DOSRAM.

Estimation conditions are as follows: the capacitor in the memory cell had 3.5fF; the voltage for judging that high data has been written was 0.52V; the power supply voltage was 3.3V; the drain voltage was 1.2V. In measurement for the estimation, −10.6V was applied to the BGE with the aim of obtaining a retention time of 10s at 192°C. The operation of writing data 1 (0.52V) into the memory with data 0 (0V), assumed as the bottleneck for the memory, was estimated from the static characteristics. The estimation results are shown in Fig. 5.

The estimated write time at 192°C is 0.49ns, demonstrating the feasibility of fast writing in high-temperature environment. An estimated retention time of 11s indicates the possibility that the DOSRAM achieves a long retention time, compared with a DRAM refresh of several tens of ms [13, 14].

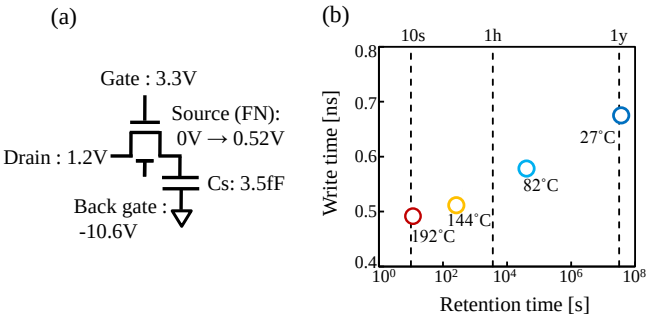

Fig. 5 (a) Conditions for DOSRAM cell using a CAAC-IGZO FET. (b) Estimated write time and retention time of DOSRAM.

5. Conclusion

We fabricated a CAAC-IGZO FET with L of 60nm and measured temperature dependence of its electrical characteristics. In high-temperature environment, the FET maintains the saturation mobility and demonstrates a high on/off ratio of drain current. The CAAC-IGZO FET will be applied to memory capable of fast writing and long-term retention under high-temperature conditions.

References

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