Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp793-794

Poly-Si Thin-Film-Transistors with Dot-Array Doping Channels Fabricated by Nano Imprint Lithography

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Abstract

In this study, we focus on the characteristics of poly-Si thin-film transistors (TFTs) with dot-array doping channels fabricated using nano imprint lithography. The array doping regions, with the dot size of about ~400nm, were fabricated by ion implantation through the PMMA mask, patterned with nano imprint technology. The proposed TFTs show lower threshold voltage, higher ON/OFF ratio, better sub-threshold swing, higher field-effect mobility, and the reduced kink-effect comparing to the conventional single channel ones. This method can be applied for the fabrication of the high-performance poly-Si TFTs in the future.

1. Introduction

Polycrystalline-silicon thin-film-transistors (poly-Si TFTs) have been the potential devices for flat-panel display applications [1-4]. The bridged-grain (BG) poly-Si TFTs, with numbers of heavily doping lines/gratings, that aimed to improve the device performance with creating a series of junctions at the channel, and building the connection of carriers at the grain boundaries for poly-Si [3-4]. The related concept had been fabricated and studied for the p-type channel poly-Si TFTs [3-4].

In this work, the n-type poly-Si TFTs with dot-array doping channels were fabricated by nanoimprint (NIL) lithography. The proposed devices were characterized and compared to those with the conventional single channel ones.

2. Device Fabrication

In this work, the n-type top-gate poly-Si TFTs were fabricated. For the starting substrate, a 500-nm thermal oxide layer was grown on (100) p-type Si and the undoped amorohous-Si, with a thickness of around 100nm, was deposited by low-pressure chemical vapor deposition (LPCVD) at 580 ºC. Then, the solid-phase crystallization (SPC) was carried out, at 600 ºC for 24 hours in N_2, to transform the amorohous-Si into a poly-Si structure. The Si mold was fabricated by E-beam lithography and reactive ion etching (RIE). The size/space of the dot-array patterns was about ~400/400 and 400/800 nm After that, the patterns were imprinted by the NIL technique with PMMA resists at 130~150 ºC and 400~500 psi. Then, the phosphorous ion implantation was performed with the dose of 1 or 2×10^{15} cm^{-2} at 25 keV. Next, the 100-nm-thick TEOS gate oxide layer and the 200-nm-thick poly-Si gate were deposited by LPCVD. After the poly-Si gate was defined, self-aligned phosphorous ion implantation to form the source/drain was performed with dose of 5×10^{15} cm^{-2} at 40 keV. The dopants were then activated by rapid thermal annealing (RTA) at 1000 ºC for 10 seconds. The 300-nm-thick passivation TEOS layer was deposited by LPCVD. Then, the contact holes were defined and Al metallization performed. Finally, the samples were sintered at 400 ºC for 30 minutes in H_2 ambient. Fabrications and the device structure of poly-Si TFTs with dot-array doping channels was shown in Fig. 1. The conventional channel TFTs were fabricated with the same mask and process steps at different regions of wafer without NIL patterns. The electrical and transfer characteristics were measured using a semiconductor parameter analyzer Agilent B1500.

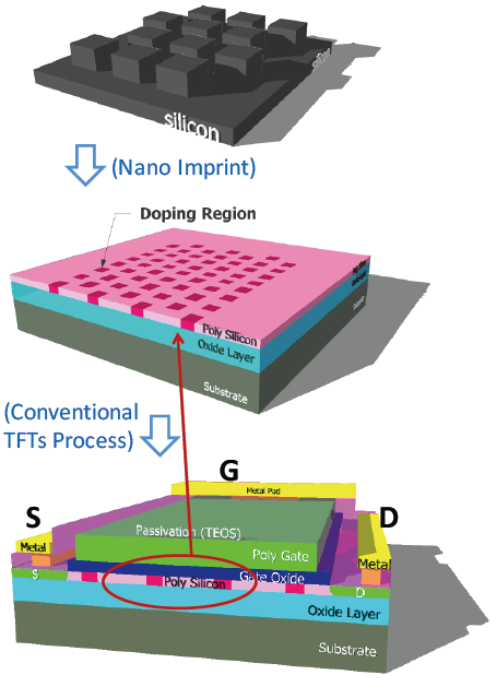

Fig. 1 Fabrications and the device structure of poly-Si TFTs with dot-array doping channels.

3. Results and Discussions

Fig. 2(a) shows the top-view OM image (50X) of poly-Si TFTs fabricated in this work; Fig. 2(b) shows the OM image (1500X) of the dot-array doping regions after ion implantation. As the figures shown, the proposed TFTs were fabricated successfully.

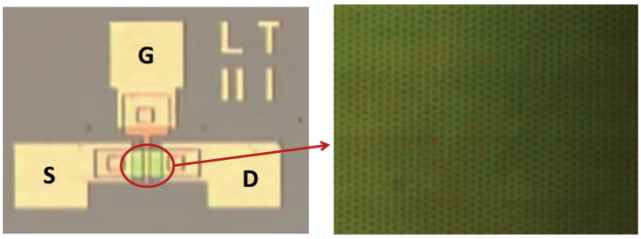

Fig. 2(a) the top-view OM image (50X) of poly-Si TFTs fabricated in this work; (b) the OM image (1500X) of the dot-array doping regions after ion implantation.

Fig. 3 compares the transfer curves, I_D-V_{GS}, of the conventional (Single) and dot-array channel (Dot) poly-Si TFTs with the implantation dose of 2×10^{15} cm^{-2}. The size/space of the dot-arrayed patterns was about ~400/400nm. The dot-array poly-Si TFTs show lower threshold voltage, better sub-threshold swing, higher drain current, and higher ON/OFF current ratio than that with a conventional single one.

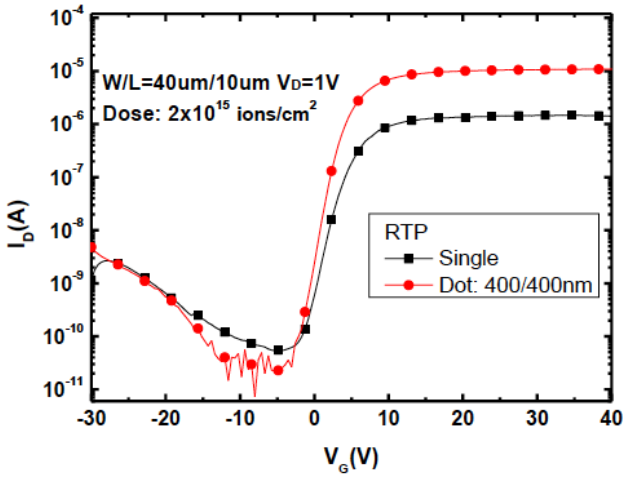

Fig. 3 The transfer curves, I_D-V_{GS}, of the conventional (Single) and dot-array channel (Dot) poly-Si TFTs with the implantation dose of 2×10^{15} cm^{-2}.

Fig. 4 compares the electrical outputs, I_D-V_{DS}, of the conventional (Single) and dot-array channel (Dot) poly-Si TFTs with the implantation dose of 2×10^{15} cm^{-2}. The size/space of the dot-array patterns was about ~400/400nm. The saturation current of dot-array poly-Si TFTs are improved, with the reduced kink effect, at high drain voltage. More detail discussions will be performed in the conference.

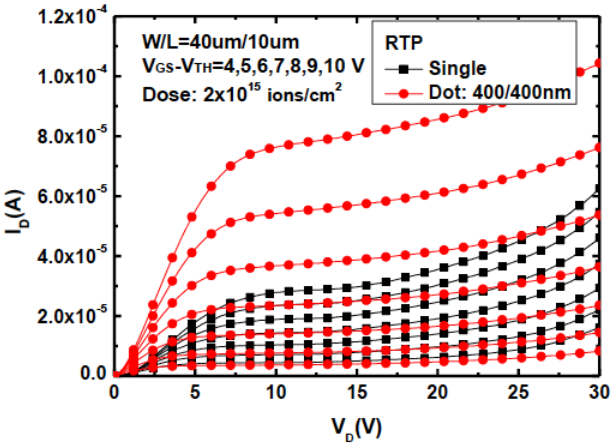

Fig. 4 The electrical outputs, I_D-V_{DS}, of the conventional (Single) and dot-array channel (Dot) poly-Si TFTs with the implantation dose of 2×10^{15} cm^{-2}.

4. Conclusions

The dot-array poly-TFTs were fabricated successfully using nano imprint technology; show lower threshold voltage, higher ON/OFF ratio, better sub-threshold swing, higher field-effect mobility, and the reduced kink-effect comparing to the conventional single ones. This technique can be applied for the fabrication of the high-performance poly-Si TFTs in the future.

Acknowledgements

The authors would like to thank the Ministry of Science and Technology, ROC (Taiwan) for financially supporting this research under Contract No. MOST 103-2221-E-260-031-MY3. The authors greatly appreciate the use of facilities at CNMM of NTHU, Hsinchu, Taiwan. Nano Device Laboratories, Hsinchu, Taiwan, is also commended for use of their facilities.

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