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Compensating for V_{TH} Variations in LTPS Thin-Film Transistors by Voltage-Programmed Pixel Circuit with Inverted OLED for AMOLED Displays

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Abstract

This work compensates for threshold voltage (V_{TH}) variations in low-temperature polycrystalline-silicon thin-film transistors (LTPS TFTs) with voltage-programmed method. The proposed 4T1C LTPS TFT-based pixel circuit avoids flicker phenomenon as it is detecting the V_{TH} of driving TFT by suppressing the cross-voltage of OLED lower than V_{TH} of OLED. It also provides the parallel addressing scheme to extend programming time for detecting V_{TH} of driving TFT completely. Simulation results demonstrate the relative current error rates are below 3.6 % and 1.7 % as the V_{TH} varies by ±0.5 V and V_{DD} drops by 0.5 V, respectively.

1. Introduction

Due to the high mobility and stability of the low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs), LTPS TFTs are commonly utilized to compose pixel circuits for high-resolution active-matrix organic light-emitting diode (AMOLED) displays [1]-[3]. However, the fabrication process variations in electrical characteristics of LTPS TFTs, such as mobility and threshold voltage (V_{TH}), leading to the non-uniformity of OLED driving currents [3]. In addition, the voltage drop in power line (V_{DD} drop) also causes non-uniformity of OLED driving currents of p-type LTPS TFTs pixel circuit [2]. To solve above issues, the current-programming method and voltage-programming method are proposed [4]. Because of the fast compensation and lower power consumption of voltage-programming method, it is commonly used to compensate for V_{TH} variations [3]. However, there is an undesirable current flow through OLED as the pixel circuit is detecting V_{TH} of driving TFT causing the flicker phenomenon [2], [5]. Moreover, due to a short scan time of a row of the high-resolution AMOLED displays, the programming time is not long enough for detecting V_{TH} of driving TFT completely [3].

Therefore, this work proposes a 4T1C pixel circuit with inverted OLED to compensate for V_{TH} variations in LTPS TFTs. It also avoids flicker phenomenon by suppressing the cross-voltage of OLED lower than V_{TH} of OLED and provides the parallel addressing scheme to extend programming time for detecting V_{TH} of driving TFT completely. Simulation results demonstrate that the relative current error rates are all below 3.6 % as the V_{TH} of driving TFT vary by ±0.5 V and below 1.7 % as V_{DD} drops by 0.5 V.

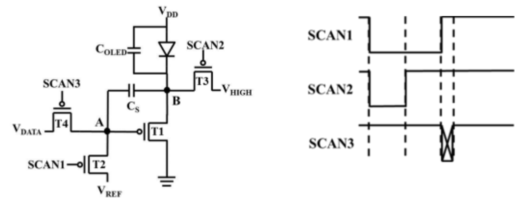


Fig. 1. Schematic and timing diagram of proposed pixel circuit.

2. Circuit Schematic and Operation

Fig. 1 shows schematic and the timing diagram of the proposed pixel circuit, which is composed of one driving TFT (T1), three switching TFTs (T2, T3 and T4), and one capacitor (C_S).

The operation of the proposed pixel circuit can be divided into four periods − reset period, programming period, data input period and emission period. During reset period, SCAN1 and SCAN2 are low to turn on T2 and T3, and SCAN3 is high to turn off T4. The reference voltage (V_{REF}) and a high voltage (V_{HIGH}) are applied to node A and node B, respectively, to reset gate voltage (V_A) and source voltage (V_B) of the driving TFT.

During the programming period, SCAN2 becomes high to turn off T3. Then V_B is discharging through T1 to yield a voltage written as,

$$V_B = V_{REF} + \left|V_{TH\_T1}\right| \tag{1}$$

where the V_{TH_T1} is the detected V_{TH} of T1 stored in C_S.

During the data input period, the SCAN1 and SCAN2 are high to turn off T2 and T3, and SCAN3 is low to turn on T4. The data voltage is applied to node A, and the V_B will be coupled by C_S and capacitor of OLED (C_{OLED}) to a lower voltage, which is expressed as,

$$V_B = V_{REF} + \left|V_{TH\_T1}\right| + (V_{DATA} - V_{REF})\frac{C_S}{C_S + C_{OLED}} \tag{2}$$

Notably, V_B in above periods are high enough to suppress cross-voltage of OLED lower than V_{TH} of OLED (V_{OLED}) to prevent currents flow through OLED to avoid the flicker.

Finally, during the emission period, SCAN1, SCAN2 and SCAN3 are high to turn off T2, T3 and T4. The V_B becomes $V_{DD}-V_{OLED}$, and the V_A is coupled to a low voltage,

$$V_A = V_{DD} - V_{OLED} - \left|V_{TH\_T1}\right| + (V_{DATA} - V_{REF})\frac{C_{OLED}}{C_S + C_{OLED}} \tag{3}$$

Therefore, OLED driving current (I_{OLED}) can be written as,

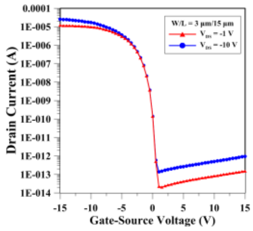
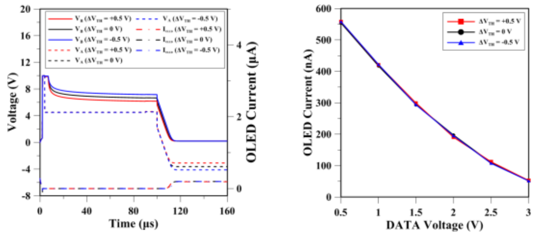


Fig. 2. Fitted transfer characteristics of LTPS TFT.



(a) (b)

Fig. 3. (a) Transient waveforms of V_A, V_B and I_{OLED} with V_{TH} variation of ±0.5 V. (b) OLED currents versus data voltages.

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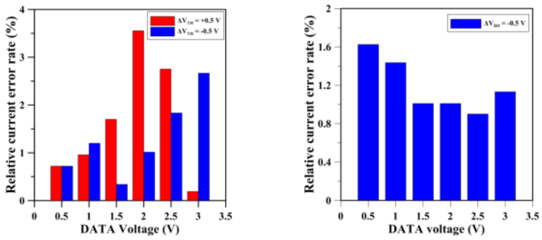
\begin{aligned}
I_{OLED} &= \frac{k_{T1}}{2}(V_B - V_A - |V_{TH\_T1}|)^2 \\
&= \frac{k_{T1}}{2}\{(V_{DD} - V_{OLED}) \\
&\quad - \left[V_{DD} - V_{OLED} - |V_{TH\_T1}| + (V_{DATA} - V_{REF})\frac{C_{OLED}}{C_S + C_{OLED}}\right] - |V_{TH\_T1}|\}^2 \\
&= \frac{k_{T1}}{2}\left[(V_{REF} - V_{DATA})\frac{C_{OLED}}{C_S + C_{OLED}})\right]^2 \qquad (4)
\end{aligned}
$$

According to Eq. (4), V_{TH_T1} and V_{DD} are eliminated to prevent I_{OLED} from influences of V_{TH} variations and V_{DD} drop.

3. Results and Discussion

The simulations are conducted using HSPICE software with LTPS TFT fitting models (LEVEL=62). The aspect ratio of T1, T2, T3 and T4 are 3 μm/15 μm, 3 μm/3 μm, 3 μm/3 μm and 3 μm/3 μm, respectively. The capacitance of C_S and C_{OLED} are 0.1 pF and 0.4 pF, respectively. The voltages of SCAN1, SCAN2 and SCAN3 are from -10 V to 10 V, and V_{DATA} ranges from 0.5 V to 3 V. V_{DD}, V_{SS}, V_{HIGH}, V_{REF}, and V_{OLED} are 6 V, 0 V, 10 V, 4.5 V, and 4 V, respectively. Fig. 2 shows the fitted transfer characteristics of the fabricated p-type LTPS TFT as the drain-source voltages are -1 V and -10 V and the gate-source voltage is set from -15 V to 15 V. Fig. 3(a) plots the transient waveforms of V_A, V_B, and I_{OLED} with V_{TH} variations of ±0.5 V. It demonstrates that the V_B are higher than $V_{DD}-V_{OLED}$ and the I_{OLED} are 0 μA in programming period indicating the OLED is maintained at off-state and no image flickering occurs. Moreover, with the parallel addressing scheme, the proposed pixel circuit applies a long programming time and detects the voltage differences of V_B as +0.5 V and -0.497 V which are close to V_{TH} variations. Furthermore, the detected voltage differences are coupled to V_A in emission period making the I_{OLED} be uniform. Fig. 3(b) plots I_{OLED} versus data voltages at entire gray level as the V_{TH} of driving TFT varies by ±0.5 V. It reveals that although the proposed pixel circuit is suffered from V_{TH} variations, the I_{OLED} are uniform at all gray levels. The relative current error rates of I_{OLED} with V_{TH} variations and V_{DD} drop are plotted in Figs. 4(a) and (b), respectively. Fig. 4(a) shows the relative current error rates are below 3.6 % as the V_{TH} of driving TFT varies by ±0.5 V. Fig. 4(b) shows the relative current error rates are all below 1.7 % as the V_{DD} drops by 0.5 V. Therefore, the simulation results confirm the compensation ability, the flicker free, and high uniformity of I_{OLED} of the proposed pixel circuit.



(a) (b)

Fig. 4. Relative current error rates of proposed pixel circuit with (a) V_{TH} variations of ±0.5 V (b) V_{DD} drop of 0.5V

4. Conclusions

A 4T1C LTPS TFT pixel circuit with inverted OLED is proposed in this work. It suppresses cross-voltage of OLED lower than V_{TH} of OLED to avoid flicker phenomenon as pixel circuit is not in emission period and extends programming time with parallel addressing scheme. Simulation results reveal that the V_{TH} of driving TFT is detected successfully and the current error rates are below 3.7 % as the V_{TH} varies by ±0.5 V and below 1.7 % as V_{DD} drops by 0.5 V.

Acknowledgements

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