Extended Abstracts of the 2018 International Conference on Solid State Devices and Materials, Tokyo, 2018, pp799-800

Solution-processed organic-inorganic perovskite thin film transistors

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Abstract

Through optimization of fabrication conditions and device architectures, we demonstrated very high hole mobilities of up to 26 cm^2 V^{-1} s^{-1} and electron mobilities of up to 4.8 cm^2 V^{-1} s^{-1} along with negligible hysteresis and good bias stability in solution-processed perovskite thin film transistors. These results lead to fabrication of high-performance perovskite-based drive and integrated circuits, sensor, and opto(electronic) devices at a lower cost in the future.

1. Introduction

While organic-inorganic perovskite materials are currently attracting considerable attention as an absorber for highly efficient solar cells, we have focused our attention on utilizing perovskite materials as the semiconductor in field-effect transistors because perovskites promise the processability and flexibility inherent to organic semiconductors as well as the excellent carrier transport inherent to inorganic semiconductors. Several reports of transistors with perovskite as the semiconductor already exist but their field-effect carrier mobilities are not sufficient for practical applications. The source of low carrier mobilities in reported perovskite transistors is thought to be low perovskite quality, high carrier trap density, and inefficient carrier injection. In addition to improving carrier mobilities, large hysteresis in output and transfer characteristics measured at room temperature is another serious issue for perovskite transistors. Thus, the true performance of perovskite transistors remains unknown and open to debate. In this study, we demonstrated high-performance perovskite transistors by solving the above-mentioned issues.

2. Results and Discussion

P-channel perovskite transistors [1]

In this study, we used the perovskite $(C_6H_5C_2H_4NH_3)_2SnI_4$ (hereafter abbreviated as $PEASnI_4$) as the semiconductor in thin film transistors because this perovskite had better transistor performance among reported perovskite semiconductors. For fabrication of perovskite transistors, we treated a silicon dioxide gate dielectric with a self-assembled monolayer containing ammonium iodide terminal groups (NH_3I-SAM). Then, we fabricated a $PEASnI_4$ film by spin-coating on NH_3I-SAM-terated substrates (see Fig. 1a).

Because NH_3I-SAM is a part of the perovskite structure, we could obtain a better-developed perovskite film by NH_3I-SAM treatment. For example, perovskite films fabricated on

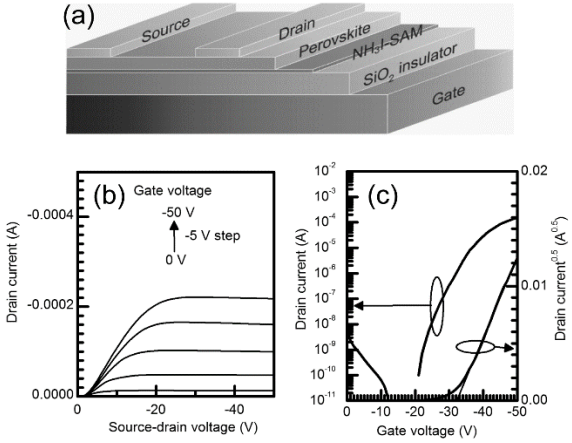

Fig. 1. (a) Fabrication of a perovskite film on a NH_3I-SAM-treated substrate. (b) Output and (c) transfer properties of *p*-channel perovskite transistors with a top-contact/top-gate architecture and NH_3I-SAM.

NH_3I-SAM had larger crystals and stronger peaks with smaller width than films without substrate treatment had. The improved morphology and crystallinity led to an increase of hole mobility from 0.53 to 2.5 cm^2 V^{-1} s^{-1} by about five-fold in a bottom-contact bottom-gate architecture with Au source/drain electrodes. Additionally, our perovskite transistors with NH_3I-SAM had negligible hysteresis in output and transfer properties because unreacted ions, the source of hysteresis, was reduced by NH_3I-SAM treatment.

We fabricated top-contact bottom-gate transistors by spin coating a $PEASnI_4$ layer on a NH_3I-SAM-treated substrate and then vacuum depositing Au source/drain electrodes on the perovskite layer through a shadow mask. This structure further increased hole mobilities to 5.7 cm^2 V^{-1} s^{-1}, probably because of improved hole injection caused by slight intermixing of the Au and perovskite layers.

The large injection barrier for holes from Au to perovskite (about 0.84 eV) results in inefficient hole injection even in a top-contact architecture. To relax the hole injection barrier, we inserted 2-nm-thick molybdenum oxide (MoO_x) hole injection layers with high work function between the Au and perovskite layers in a top-contact/bottom-gate architecture, increasing hole mobilities to 7.1 cm^2 V^{-1} s^{-1}.

The bulk resistance on the path between the source/drain electrodes and the channel in a top-contact/bottom-gate structure reduces transistor performance but can be absent in a top-

contact/top-gate architecture. Taking advantage of the improved hole injection and the absence of bulk resistance, we further increased hole mobilities by fabricating top-contact/top-gate transistors with a CYTOP gate dielectric layer and MoO_x hole injection layers. This structure resulted in a further increase of hole mobility up to 15 $cm^2\ V^{-1}\ s^{-1}$. A smaller carrier trap density at a $PEASnI_4$/CYTOP interface, evaluated by a thermally stimulated current method, is another reason for the improved transistor properties. Figure 1b and 1c are examples of our perovskite transistor properties.

N-channel transistors [2]

Large electron injection barriers and electrode degradation are serious issues that need to be overcome to obtain *n*-channel operation in thin film transistors with a $PEASnI_4$ semiconductor. By employing low-work-function Al source/drain electrodes and by inserting C_{60} layers between $PEASnI_4$ and Al to reduce the injection barrier and to suppress the electrode degradation, we demonstrate *n*-channel perovskite transistors with electron mobilities of up to 2.1 $cm^2\ V^{-1}\ s^{-1}$. Grazing-incidence X-ray scattering and thermally stimulated current measurements revealed that crystallite size and electron traps largely affect the *n*-channel transport properties.

Contact resistance [3]

The performance of transistors with a $PEASnI_4$ semiconductor is strongly limited by the presence of the contact resistance. To evaluate the intrinsic carrier mobilities, we fabricated *p*- and *n*-channel perovskite transistors with large channel lengths. Field-effect hole and electron mobilities gradually increased and threshold voltage decreased as channel lengths were increased and then became constant in a large-channel length region (Fig. 2). This is because of the reduced contribution of the contact resistance relative to the total resistance. The intrinsic carrier mobilities estimated from this region reached 26 and 4.8 $cm^2\ V^{-1}\ s^{-1}$ for holes and electrons, respectively, which are the highest ever reported in any perovskite transistor.

Air Stability

Our $PEASnI_4$ transistors were very stable under electrical bias in vacuum but were very sensitive to oxygen; a very quick degradation of transistor performance by oxidation. With the aim of realizing air-stable perovskite transistors, we optimized perovskite fabrication conditions. As the results, we obtained improved air stability in top-contact/bottom-gate transistors by about two-fold. Moreover, we encapsulated a perovskite semiconductor with a CYTOP polymer film by spin-coating. These encapsulated transistors had almost unchanged transistor properties over 5 h of exposure to air.

3. Conclusions

In summary, we have demonstrated very high hole and electron mobilities of up to 26 and 4.8 $cm^2\ V^{-1}\ s^{-1}$, respectively, in $PEASnI_4$ transistors. Here, we would like to discuss

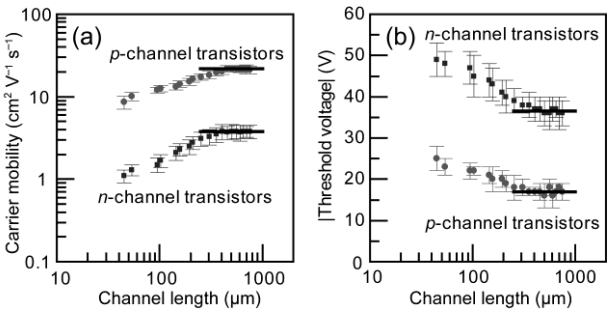

Fig. 2. Plots of (a) carrier mobilities and (b) threshold voltages as a function of channel length for *p*- and *n*-channel perovskite transistors.

the remaining issues, which must be overcome to further develop $PEASnI_4$ transistors. In this study, we employed large channel length to increase hole mobility. However, large channel length is disadvantageous to practical applications. Therefore, we need to reduce contact resistance even at small channel length through source/drain electrode modification. In our previous study, we roughly estimated the crystallite size of a spin-coated $PEASnI_4$ film to be 30–35 nm from a width of X-ray diffraction peaks using Scherrer equation. Compared with the channel length used here, the estimated crystallite size is much smaller, indicating that the carrier transport would be strongly limited by crystallite-crystallite boundaries. An increase of crystallite size by optimizing $PEASnI_4$ film fabrication conditions could lead to the enhancement of transistor performance. We analyzed a spin-coated $PEASnI_4$ film by X-ray photoelectron spectroscopy to estimate its atomic ratio. The estimated atomic ratio was Sn : N : I = 1 : 1.7 : 3.7 whereas the ideal ratio is Sn : N : I = 1 : 2 : 4. This may mean that the organic component $C_6H_5C_2H_4NH_3I$ is lacking relative to the inorganic component SnI_2 although a precursor solution used for spin-coating contained a stoichiometric ratio (1:2). This non-stoichiometry is expected to result in lower perovskite film quality and transistor performance because unreacted SnI_2 works as carrier scattering centers. Therefore, there is room to improve transistor performance if we can fabricate a stoichiometric $PEASnI_4$ film by, for example, spin-coating from a non-stoichiometric solution with a higher organic concentration. We are now investigating to overcome the above issues in our laboratory with the aim of realizing carrier mobilities > 100 $cm^2\ V^{-1}\ s^{-1}$ in solution-processed perovskite transistors.

Acknowledgements

This work was supported by JSPS KAKENHI, grant numbers JP15K14149 and JP16H04192 and Canon foundation.

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