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Effect of Tin and Gallium Composition on the Instability of Amorphous Indium-Gallium-Zinc-Tin-Oxide (IGZTO) Thin-Film Transistors under Positive Gate Bias

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Abstract

The effect of Sn and Ga composition in the amorphous IGZTO on the instability of the Thin-Film Transistors (TFTs) under positive gate bias was investigated. The sample with a highest Sn and Ga composition showed a largest positive threshold voltage shift (ΔV_{th}). As Sn and Ga composition was reduced, the positive ΔV_{th} was suppressed and the sample with a lowest Sn and Ga composition showed a negative ΔV_{th}. This different V_{th} shift behavior can be explained by a trap model that both donor-like Gaussian states and accepter-like tail states exist in IGZTO film. And it was revealed that the Sn and Ga composition strongly affect these two kinds of states and turn out to be the key nob to improve the positive bias instability.

1. Introduction

During the past few years, **I**ndium **G**allium **Z**inc **O**xide (IGZO) TFTs has attracted much interest as BEOL transistors for 3D-LSI applications for their extremely low off-state current and low-temperature fabrication process [1-2]. On the other hand, **I**ndium **T**in **Z**inc **O**xide (ITZO) and **I**ndium **G**allium **Z**inc **T**in **O**xide (IGZTO) have been reported to show higher mobility than IGZO [3-5], but the effects of the Sn and Ga composition of IGZTO on the electrical characteristics of IGZTO have not been reported. Since reliability of TFTs is one of the most important issues for their mass production, we investigated the effects of the metal cation composition of IGZTO on the device reliabilities, such as temperature dependence and instability under positive gate bias stress.

2. Experimental

The cross-sectional view of the IGZTO TFT used is shown in Fig.1. MoTa and Mo were used for gate and source/drain (S/D) electrodes, respectively. SiO_2 deposited by PECVD was used for gate insulator and etch stopper layer with a thickness of 40 nm and 150 nm, respectively. The IGZTO active layer with a thickness of 15 nm was deposited by sputtering. Four samples (A, B, C, D) with different cation composition of the IGZTO film were fabricated by using different IGZTO target. Ga and Sn composition in four IGZTO films showed following relationship: A>B>C>D. After TFT fabrication, all samples were annealed for 30 min at 300 ^{o}C in N_2 ambient. The devices used have dimensions of channel width/length =2μm/2μm.

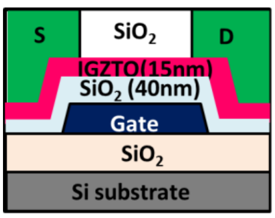

Fig.1. Cross-sectional view of the IGZTO TFT.

Firstly, the I_d-V_g characteristics at various temperatures ranging from 25 ^{o}C to 85 ^{o}C of the IGZTO TFTs without stressing were measured. The threshold voltage (V_{th}) was defined as the gate voltage when the drain current reaches 10^{-11} A. Constant positive gate bias ($V_g = V_{th0} + 20$V) stress measurements were performed for a period of 1000s at various temperature with the source and drain grounded. Here V_{th0} was defined as the V_{th} before stressing test.

3. Results and Discussion

Fig.2 shows V_{th0} extracted from the I_d-V_g characteristics before stressing as a function of temperature. Although as Sn and Ga composition was reduced, V_{th0} was slightly decreased, V_{th0} for all samples were in the range of 0±0.1V at 25 ^{o}C and V_{th0} linearly decreased with temperature with a temperature coefficient of 4 mV/^{o}C. This can be explained by the larger concentration of free carriers available, which exited from localized states as temperature is increased [6].

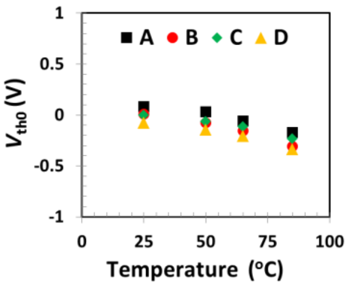

Fig.2. Temperature dependence of V_{th0} of IGZTO TFTs before stressing.

Fig.3 (a)~(d) show ΔV_{th} as a function of stress time at various temperature for sample A~D respectively. For sample A, B and C, V_{th} shifted to a positive V_g direction and ΔV_{th} increased with increasing the stress time and temperature when temperature was below 65 ^{o}C. However, ΔV_{th} firstly increased and then reduced for sample B and C when temperature was 85 ^{o}C. On the other hand, sample D showed an opposite tendency compared to sample A: V_{th} of sample D shifted to a negative V_g direction and the absolute value of ΔV_{th} increased with increasing the stress time and temperature. Fig.4 (a)~(b) show Ga and Sn composition dependence of ΔV_{th}: A comparison of four samples at stress time, t=100 and 1000s, respectively. We can see that ΔV_{th} was strongly affected by Ga and Sn composition. Within t = 1000s, sample A with a highest Sn and Ga composition showed a largest positive ΔV_{th}. As Sn and Ga composition was reduced, positive ΔV_{th} was suppressed and sample D with a lowest Sn and Ga composition showed a negative ΔV_{th}.

Based on previous research, the origin of a positive ΔV_{th} of IGZO TFTs under positive bias stress tests can be explained by two models: charge trapping and defect creation [7].The transfer characteristics of sample A, B and C under bias stress tests when temperature was below 50 ^{o}C almost exhibited parallel shifts, and the observed changes in subthreshold slope, *S*, as shown in Fig 5, were small. On the other hand, the device recovered after relaxation without any annealing, here, the measured transfer characteristics of sample B before, under stress and during recovery at 50 °C are shown in Fig.6 as a typical example. All the above results suggest that charge trapping is believed to be the main mechanism responsible for the observed positive ΔV_{th}. In our study, four samples had a same structure and the only difference was the composition of the IGZTO channel. Thus, we speculated that the different positive ΔV_{th} among samples were most likely due to the difference of contribution of electron trapping within the IGZTO channel layer and/or near the channel/dielectric interface.

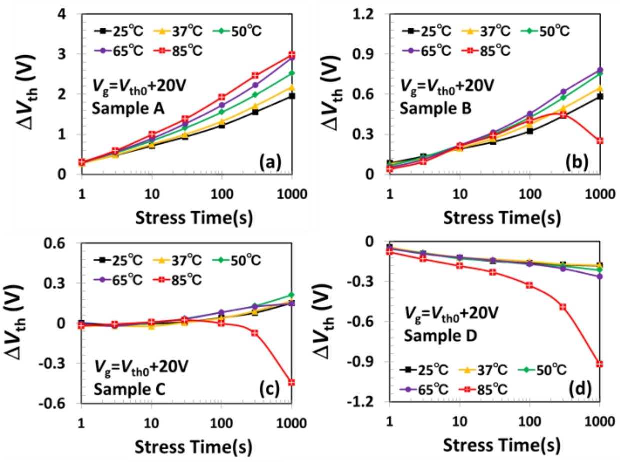

Fig.3. ΔV_{th} as a function of stress time at various temperature ranging from 25 °C to 85 °C for a constant positive gate bias stress test, in which V_g=V_{th0}+20V with the source and drain grounded.

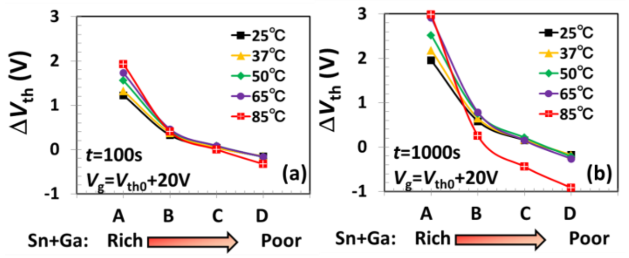

Fig.4. Relationship between ΔV_{th} and Sn and Ga composition in IGZTO at various temperature ranging from 25 °C to 85 °C.

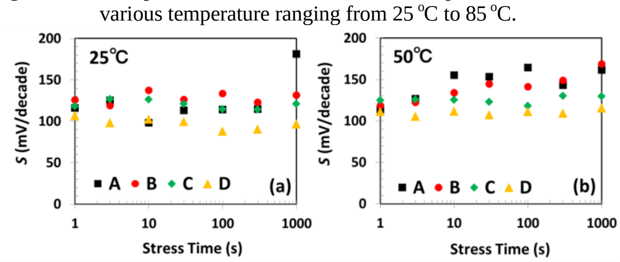

Fig.5. *S* factor as a function of stress time, which was almost not affected under bias stress when temperature was below 50 °C.

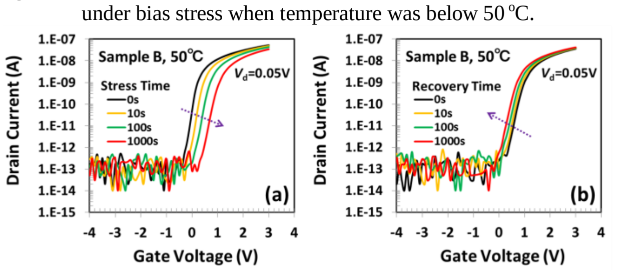

Fig.6. Transfer characteristics of sample B as a typical example measured at 50 °C as a function of (a) stress time and (b) recovery time after stress.

Fig.7 shows schematic illustration of the subband-gap density of states (DOS) in our IGZTO film. It consists of the acceptor-like tail states, the donor-like tail states and the donor-like Gaussian states. Since Sn-O (528 kJ/mol) and Ga-O (374 kJ/mol) have a larger bond dissociation energy than In-O (346 kJ/mol) and ZnO (<250 kJ/mol), a higher Ga and Sn composition can result in a higher density of acceptor-like states, causing more electrons to be trapped under bias, thus lead to a larger positive V_{th} shift.

On the other hand, for sample D, which had a lowest density of acceptor-like states, acceptor-like states were fully occupied and free carriers, which exited from donor-like Gaussian states, became more under bias, as a result, V_{th} shifted to a negative direction. For sample B and C, which had a higher density of acceptor-like states than that of sample D, acceptor-like states were not fully occupied at low temperature, and could be fully occupied at high temperature by the larger amount of electrons exited from donor-like Gaussian states after a certain stress time, then the extra electrons became free carriers, as a results, V_{th} first shifted to a positive direction and then to a negative direction.

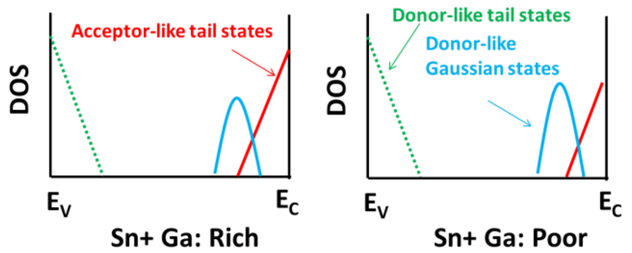

Fig.7. Schematic illustration of the subband-gap DOS in IGZTO, which consists of the acceptor-like tail states, the donor-like tail states and the donor-like Gaussian states. A higher Ga and Sn composition can cause a higher density of acceptor-like states and a lower density of donor-like Gaussian states.

4. Conclusion

In this study, we have investigated the positive bias stress induced V_{th} instabilities in amorphous IGZTO TFTs with varying Sn and Ga composition in IGZTO films. The stability was highly dependent on the cation composition. Sample A with a highest Sn and Ga composition showed a largest positive ΔV_{th}. As Sn and Ga composition was reduced, the positive ΔV_{th} was suppressed and sample D with a lowest Sn and Ga composition showed a negative ΔV_{th}. From the transfer characteristics measured before, under stress and during recovery, the charge trapping phenomenon in the IGZTO channel layer, which consists of the acceptor-like tail state and the donor-like Gaussian state, is considered as the main cause of ΔV_{th} and Sn and Ga composition can strongly affect these two kinds of states. By optimizing the metal cation composition, IGZTO semiconductor system can be a promising candidate for TFTs with excellent stability as well as high performance.

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